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Failure Mechanisms and Models for Semiconductor Devices

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FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

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FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

Foreword

This publication provides guidance in the selection of reliability modeling parameters, namely functional form, apparent thermal activation energy values, and sensitivity to stresses such as power supply voltage, substrate current, current density, gate voltage, relative humidity, temperature cycling range, mobile ion concentration, etc.

The failure mechanisms described in the several sections of this publication constitute commonly accepted industrial models, validated by a team of reliability experts (SEMATECH/ISMI Reliability Council) and buttressed by citations to the most cogent published literature.

Revisions have been made to reflect technology changes, especially as Cu now supplements Al and low-dielectric-constant insulators are complementing traditional silica.

Introduction

Accelerated tests are typically used to find and identify potential failure mechanisms in semiconductor devices and to estimate the rate of their occurrence in electronic systems. The historical approach to investigating the relationship between a maximum stress failure rate and a system failure rate is to choose a single representative "equivalent" apparent thermal activation energy for a given product or product group. A single, best-estimate apparent activation energy value facilitates accurate estimation of the acceleration factor for the device failure rate estimation in the system application.

A word about formats within this document: parentheses **( )** enclose equation numbers; square brackets **[ ]** enclose citation numbers. All equation, citation, and figure numbers include the subclause number so that individual clauses can be modified without disturbing other clauses, except for page numbers. Thus, **(5.3.2)** is the 2nd equation in 5.3 and **[5.11.5]** is the 5th citation in 5.11. The citations can be found in Annex A.

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

(From JEDEC Board Ballot JCB-01-97, JCB-03-39, JCB-08-61, JCB-09-19, JCB-10-64, JCB-11-74, and JCB-16-32, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum-of-the-Failure-Rates method.

The models apply primarily to the following:

a) Aluminum (doped with small amounts of Cu and/or Si) and copper alloy metallization

b) Refractory metal barrier metals with thin anti-reflection coatings

c) Doped silica or silicon nitride interlayer dielectrics, including low-dielectric-constant materials

d) Poly silicon or “salicide” gates (metal-rich silicides such as W, Ni & Co to decrease resistivity)

e) Thin SiO_2 gate dielectric

f) Silicon with p-n junction isolation

g) Tin Whisker Growth Kinetics

h) Printed Circuit Board Ionic Mobility

2 Terms and definitions

For the purpose of this publication, the following terms and definitions apply.

acceleration factor (*A*, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann’s constant in electronvolts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used in place of the symbol *A*.

acceleration factor, stress (A_f): The acceleration factor due to the presence of some stress (e.g., current density, electric field, humidity, temperature cycling).

2 Terms and definitions (cont'd)

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature.

NOTE 1 This is the acceleration factor most often referenced. The Arrhenius equation for reliability is commonly used to calculate the acceleration factor that applies to the acceleration of time-to-failure distributions for microcircuits and other semiconductor devices:

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp[(-E_{aa}/k)(1/T_1 - 1/T_2)] \quad \textbf{(2.1)}$$

where

E_{aa} is the apparent activation energy (eV);
k is Boltzmann's constant (8.62×10^{-5} eV/K);
T_1 is the absolute temperature of test 1 (K);
T_2 is the absolute temperature of test 2 (K);
λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});
λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1}).

NOTE 2 The best-fit linear slope of a plot of the natural log of the time-to-failure as a function of $1/k$T, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is equal to the apparent activation energy in electronvolts.

NOTE 3 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s.

activation energy (E_a): The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur.

NOTE The activation energy is used in the Arrhenius equation for the thermal acceleration of physical reactions. The term "activation energy" is not applicable when describing thermal acceleration of time-to-failure distributions, e.g., in the Arrhenius equation for reliability; hence the need for the term "apparent activation energy".

apparent activation energy (E_{aa}): An energy value, analogous to activation energy, that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions.

NOTE 1 An apparent activation energy should be associated with a specific failure mechanism and an observed time-to-failure distribution to calculate the acceleration factor for converting the observed failure rate to the quoted failure rate at a different temperature.

NOTE 2 An activation energy is a measure of the heat energy needed to establish the rate of reaction for a specific failure mechanism. The reaction rate and other contributing factors, e.g., radiation, voltage, humidity, magnetic fields, determine the unique time-to-failure distribution for the modeled failure mechanism.

NOTE 3 The apparent activation energy is empirically determined from the change in an observed time-to-failure distribution with temperature.

bathtub curve: A plot of failure rate versus time or cycles that exhibits three phases of life: infant mortality (decreasing failure rate), intrinsic or useful life (relatively constant failure rate), and wear-out (increasing failure rate).

Boltzmann's constant (k): A constant equal to 1.38×10^{-23} joule per kelvin or 8.62×10^{-5} electronvolt per kelvin.

2 Terms and definitions (cont'd)

cumulative distribution function of the time-to-failure; cumulative mortality function [F(*t*)]: The probability that a device will have failed by a specified time t_1, or the fraction of units that have failed by that time.

NOTE 1 The value of this function is given by the integral of f(*t*) from $t = 0$ to $t = t_1$ and is generally expressed in percent (%) or in parts per million (ppm) for a defined early-life failure period. See "probability density functionof the time-to-failure" for f(*t*).

NOTE 2 The abbreviation CDF is often used; however, the symbol F(*t*) is preferred.

cumulative hazard function [H(*t*)]: The fraction of units that have failed referenced to the survivors (not to the initial number of units).

NOTE The value of this function at a specified time t_1 is given by the integral of h(*t*) from $t = 0$ to $t = t_1$. See "instantaneous failure rate; hazard rate" for h(*t*).

cumulative reliability function [R(*t*)]: The probability that a device will still be functional at a specified time t_1, or the fraction of units surviving to that time.

NOTE R(*t*) = 1 – F(*t*). See "cumulative distribution function of the time-to-failure" for F(*t*).

failure mechanism: The physical, chemical, electrical, or other process that has led to a nonconformance.

NOTE 1 See JESD671, Component Quality Problem Analysis and Corrective Action Requirements.

NOTE 2 A failure mechanism may be characterized by how a degradation process proceeds including the driving force, e.g., oxidation, diffusion, electric field, current density. When the driving force is known, a mechanism may be described by an explicit failure rate model; identifying that model with associated parameters is the main objective of this document.

failure mode: (general) The way in which a failure mechanism manifests itself in a failing component.

NOTE 1 Examples of failure modes are a visual blemish, a bent lead, a foreign particle or material, an incorrect dopant profile or grain size, a scratch, an electrical fault (open, short, leakage, inadequate slew rate or noise margin, stuck at high or low, etc.).

NOTE 2 Failure rate distributions for a given failure mode can be modeled only when the failure mechanism and the relevant independent variables (forcing functions) are known.

failure rate (*λ*): The fraction of a population that fails within a specified interval, divided by that interval.

NOTE 1 Standard methods of reporting failure rates of semiconductor devices include 1) percent failed per 1000 hours and 2) FITs.

NOTE 2 The interval may be expressed in operating hours, storage hours, operating cycles, or other units of interval measurement.

NOTE 3 Typically, the term "failure rate" means the instantaneous failure (hazard) rate.

NOTE 4 The statistical upper limit estimate of the failure rate is usually calculated using the χ^2 (chi-squared) function.

failures in time (FITs): The number of failures per 10^9 device hours.

2 Terms and definitions (cont'd)

instantaneous failure rate; hazard rate [h(*t*)]: The rate at which devices are failing referenced to the survivors (not to the initial number of units).

NOTE h(*t*) = f(*t*)/R(*t*). See "probability density function of the time-to-failure" for f(*t*) and "cumulative reliability function" for R(*t*).

mean-time-between-failures (MTBF): The average time between failures in repairable or redundant systems.

mean-time-to-failure (MTTF): The average time to failure for components or nonrepairable systems.

NOTE The MTTF is often the reciprocal of the hazard rate when the hazard rate is described by the Poisson or equivalent exponential function, e.g., in the constant or flat portion of the useful life region of the bathtub curve.

whisker: A spontaneous columnar or cylindrical filament, usually of monocrystalline metal, emanating from the surface of a finish.

NOTE Whiskers are not to be confused with dendrites, which are fern-like growths on the surface of a material, formed as a result of electromigration of an ionic species or during solidification.

observed failure rate: The failure rate determined from a product or test vehicle subjected to an accelerating stress that may produce failures attributable to one or more failure mechanisms.

PCB component cleanliness: The absence of chemical residues, on or in the surface of components on printed circuit boards, that result from their processing and handling.

NOTE These residues may react with the environmental moisture or processing conditions and have either positive or negative impact on product performance.

planning activation energy (E_{ap}): A psuedo apparent activation energy, derived from Pareto analysis and experience, using the principles of the physical relationship between stress and failure rate.

NOTE 1 E_{ap} can be used to estimate sample sizes and test times.

NOTE 2 The planning activation energy cannot be calculated as the average value of the apparent activation energies of the various failure mechanisms because different failure mechanisms have different weighting factors and the apparent activation energy values affect the acceleration factor exponentially rather than linearly.

potential physical failure mechanism: A physical failure mechanism that (1) has been identified through physical experimentation to exist for similar products or (2) can be linked to these products through the scientific study of the product (process) physical characteristics and the physical requirement found to be necessary for the failure mechanism to occur.

printed circuit board (PCB): A board for mounting of components, on which most connections are made by printed circuitry (Ref. IEEE 100).

NOTE A printed circuit board (PCB) is also known as a printed wiring board (PWB) (Ref. JEDEC JS9703).

probability density function of the time-to-failure [f(*t*)]: The distribution of the probabilities of failure as a function of time.

NOTE The probability of failure during the interval Δt that immediately follows the instant t_1 is given by the integral of f(*t*) from t_1 to ($t_1 + \Delta t$).

2 Terms and definitions (cont'd)

quoted failure rate: The predicted failure rate for typical operating conditions.

NOTE The quoted failure rate is calculated from the observed failure rate under accelerated stress conditions multiplied by an accelerated factor; e.g., $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s. When multiple failure mechanisms and thus multiple acceleration factors are involved, then a proper summation technique, e.g., sum-of-the-failure rates method, is required.

random defect: A physical defect that is correlated to some known process, equipment, or procedure, and can be described by a probability-density function of time or location.

relative humidity (RH): The ratio of the amount of water vapor in the air to the maximum amount of water vapor that volume of air can hold at that temperature and pressure.

NOTE RH is calculated as the quotient of the vapor density (or vapor pressure) in the air and the value of saturated vapor density (or saturated vapor pressure) at that specific temperature and pressure.

time-to-whisker-nucleation (TTWN): The incubation time before whiskers begin to grow.

useful life: The phase in the life of a device during which the hazard rate is relatively constant.

NOTE As typically used with the bathtub curve, the useful life phase is the bottom of the curve.

wearout: The phase in the life of a device during which the mortality function is increasing.

NOTE As typically used with the bathtub curve, the wearout phase follows the useful life of the device.

3 Inclusions, deliberate omissions, and resources

A reader may easily notice that some important issues are not treated in this document. This section is intended to show our rationale for picking what was included, what was not included, and provide references to relevant JEDEC documents.

3.1 What is included

One can readily see in Section 5 which failure mechanisms are covered in this document. The failure mechanisms were sorted in roughly a semiconductor process flow from silicon to a packaged device: Front End of Line (FEoL), Back End of Line (BEoL), and Packaging/Interfacial failure mechanisms. Only failure mechanisms, for which understanding is relatively mature, are included. Also included are sections on Statistics & Modeling Parameter Determination.

3.2 What is not included

Conspicuous by their absence are several failure mechanisms: namely those active for high-dieletric-constant gate materials (TDDB and carrier mobility) and "metal" gates, other nonvolatile memory technologies (magnetic, cross bar, ferroelectric, etc.), mechanical shock, Single Event Upsets or Soft Error Rate (SEU or SER), ESD/EOS (ElectroStatic Discharge and Electrical OverStress) which might be measured by HBM (Human Body Model) or CDM (Charged Device Model) and Latch-Up (LU).

3 Inclusions, deliberate omissions, and resources (cont'd)

3.2 What is not included (cont'd)

High-dielectric-constant materials are under active development and proliferation. The best of the candidates appear to be rare earth oxides (commonly Hafnium) or silicates, sometimes nitrided, but there are still several possibilities and several possible (poorly characterized) reliability failure mechanisms.

Metal gates are also in a considerable state of flux. "Metal" in this context can mean a conductive nitride and is in contrast to the traditional polycrystalline silicon gate. That there might be two different metal gates for a given high-dielectric-constant gate (one work function for n-type, but a different work function for p-type) adds considerable complexity to characterization and modeling of the relevant failure mechanisms.

New nonvolatile memory materials and architectures are likely in the near future, but existing Si-gate CMOS can scale a little further along the ITRS before the industry would be forced to supplant traditional technology with something completely new. Naturally, there are many unknown factors in process optimization and in reliability modeling for something completely new.

JEDEC document JESD89A shows how one should measure the failure rate for SEU. However, this document doesn't show a reader how to compute an acceleration factor (AF), which is the primary focus of this document. In principle, an SEU acceleration factor would simply be the ratio of the fluxes between one condition and the other.

One could use JEDEC JESD22-A114 or JESD22-C101 to measure vulnerability to ESD, but neither of these documents shows a method to calculate an acceleration factor. Indeed, it may not be possible to calculate an AF for a periodic stress such as ESD. Furthermore, the current state of knowledge does not allow one to compute cumulative damage leading to failure from some number of sub-lethal pulses. Similarly, we would submit that the physics are not well characterized to the point where current, current density, voltage, electric field, stress duration, etc. could be combined into a stress intensity for AF determination.

JESD78A is the JEDEC standard for a methodology to estimate LU sensitivity. The failure mechanisms created during a LU event can look like those caused by ESD or EOS. Generally, issues related to LU are best corrected through proper characterization during process development and implementation of strict design rules and methodologies associated with LU prevention. JESD78A, like the ESD standards, does not utilize an acceleration factor.

As these issues become mature and relevant, it is our intention to include them in this document.

3.3 JEDEC resources

JESD22-A101	Steady State Temperature Humidity Bias Life Test
JESD22-A103	High Temperature Storage Life
JESD22-A104	Temperature Cycling
JESD22-A105	Power and Temperature Cycling
JESD22-A106	Thermal Shock
JESD22-A108	Temperature, Bias, and Operating Life
JESD22-A110	Highly Accelerated Temperature and Humidity Stress Test (HAST)
JESD22-A113	Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing
JESD22-A114	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

3 Inclusions, deliberate omissions, and resources (cont'd)

3.3 JEDEC resources (cont'd)

JESD22-A117	Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test
JESD22-A118	Accelerated Moisture Resistance - Unbiased HAST
JESD22-A119	Low Temperature Storage Life
JESD22-A120	Test Method For The Measurement Of Moisture Diffusivity And Water Solubility In Organic Materials Used In Integrated Circuits
JESD22-A121	Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes
JESD22-B102	Solderability
JESD22-B105	Lead Integrity
JESD22-B112	High Temperature Package Warpage Measurement Methodology
JESD22-B115	Solder Ball Pull
JESD22-B116	Wire Bond Shear Test
JESD22-B117	Solder Ball Shear
JESD22-C101	Field-Induced Charged-Device Model Test Method For Electrostatic Discharge Withstand Thresholds Of Microelectronic Components
JESD28-1	N-Channel MOSFET Hot Carrier Data Analysis, (Addendum to JESD28)
JESD28	Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress
JESD33-B	Standard Method For Measuring And Using The Temperature Coefficient Of Resistance To Determine The Temperature Of A Metallization Line
JESD35-1	General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics, (Addendum No. 1 to JESD35)
JESD35-2	Test Criteria for the Wafer-Level Testing of Thin Dielectrics, (Addendum No. 2 to JESD35)
JESD35	Procedure for the Wafer-Level Testing of Thin Dielectrics
JESD60	A Procedure For Measuring P-Channel Mosfet Hot-Carrier-Induced Degradation At Maximum Gate Current Under Dc Stress
JESD61	Isothermal Electromigration Test Procedure
JESD63	Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature
JESD78	IC Latch-Up Test
JESD87	Standard Test Structures for Reliability Assessment of AlCu Metallizations with Barrier Materials
JESD88	Dictionary of Terms for Solid State Technology
JESD89-1	Test Method For Real-Time Soft Error Rate
JESD89-2	Test Method For Alpha Source Accelerated Soft Error Rate (SER)
JESD89-3	Test Method for Beam Accelerated Soft Error Rate
JESD89	Measurement And Reporting Of Alpha Particle And Terrestrial Cosmic Ray Induced Soft Errors In Semiconductor Devices

3 Inclusions, deliberate omissions, and resources (cont'd)

3.3 JEDEC resources (cont'd)

JESD90	A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities
JESD92	Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics,
JESD201	Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finished
JEP119	A Procedure For Executing Sweat
JEP139	Guideline For Constant Temperature Aging To Characterize Aluminum Interconnect Metallizations For Stress-Induced Voiding
J-STD-020	Joint IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices
JP002	Current Tin Whiskers Theory and Mitigation Practices Guideline
IPC 610	PCB Inspection Criteria

4 The basic thermal acceleration equation

When estimating acceleration due to temperature, it is customary to use the expression in equation **(2.1)**. It is an adaptation of the Arrhenius equation and has been used to express both a single failure mechanism's sensitivity to temperature (i.e., its acceleration factor) and also a product's thermal acceleration factor. By measuring parametric change caused by temperature, activation energy in its physical sense can be estimated. When used to estimate the reliability of a product, as shown in equation **(4.1)**, it is also being used to express that product's reliability with respect to temperature and as a function of time.

$$\lambda_{Top} = \lambda_{Tst} / A_T = \lambda_{Tst} / \exp[(-E_{aa} / k)(1 / T_{st} - 1 / T_{op})] \qquad \textbf{(4.1)}$$

where

λ_{Top} is the observed failure rate at an operating temperature T_{op} (h^{-1})
λ_{Tst} is the observed failure rate at stress temperature T_{st} (h^{-1})
E_{aa} is the apparent activation energy in electronvolts (eV)
k is Boltzmann's constant (8.62×10^{-5} eV/kelvin)
T_{st} is the absolute temperature of the stress in kelvins
T_{op} is the absolute temperature of an operating condition in kelvins

Equation **(4.1)** (same as 2.1) must be used with caution because this relationship holds only for systems in which the failure rate is constant. However, very few practical situations exist in which the failure rate is truly constant. Nevertheless, the assumption of constant failure rate is still commonly used. An "apparent" activation energy, E_{aa}, may be used for product failure rate estimates in the absence of extensive failure analysis based on root cause and responsible failure mechanisms.

5 Models for common failure mechanisms

The failure mechanisms described in the several sections of this standard constitute commonly accepted industrial models, validated by a team of reliability experts (from the SEMATECH/ISMI Reliability Council) and buttressed by citations to the most cogent published literature.

5.1 FEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – Gate Oxide

Time-Dependent Dielectric Breakdown (TDDB) is an important failure mechanism in ULSI devices. The dielectric fails when a conductive path forms in the dielectric, shorting the anode and cathode. It should be noted that TDDB for intermetal diectric is discussed in 5.7. It is important to make a distinction between the empirical models and the physical models developed to explain these empirical models. The experimental data can generally be described by one of four models (see citations **[5.1.1 to 5.1.12]** for historically significant papers):

1) E model or constant field/voltage acceleration exponential model
2) 1/E model or, equivalently, anode hole injection model
3) V model, where failure rate is exponential with voltage
4) Anode hydrogen release for the power-law model

The physical models used to explain the four empirical models are: A) thermo-chemical model, B) anode hole injection, C) bulk trap generation, and D) anode hydrogen release model. While the thermo-chemical and V models adopt the assumption of field-driven mechanism, both anode hole injection and anode hydrogen release models assume a current-driven mechanism in addition to the role of applied voltage or oxide fields depending on the specific conditions.

5.1.1 Constraints and limitations

These models are intended for application to SiO_2 gate dielectric over a large range of oxide thicknesses. Models and parametric values to effectively model “high-k” oxides (based on materials or composites other and silica) are unknown so these materials are not yet treated in this document.

Controversies regarding these models still exist, hence users are encouraged to review literature before they make their own decisions for their unique technologies.

5.1.2 Models

5.1.2.1 E model [5.1.3 to 5.1.16]

In the E model for gate oxide thickness greater than 4 nm, the cause of low electric field (<10 MV/cm) TDDB is due to field-enhanced thermal bond breakage at the silicon-silica interface. The E-field serves to reduce the activation energy required for thermal bond breakage and therefore exponentially increases the reaction rate for failure. The time-to-failure (TTF), inverse to reaction rate, decreases exponentially with temperature:

$$TTF = A_o * \exp(E_{aa} / kT) = TTF = A_o * \exp(-\gamma(T)\, E_{ox}) * \exp(E_a / kT) \quad \textbf{(5.1.1)}$$

where

A_o = arbitrary scale factor, dependent upon materials & process details

γ = field acceleration parameter in cm/MV, is temperature dependent, γ (T) = a / kT where a is the effective dipole moment for the molecule (see also the note at the end of this clause)

E_{ox} = externally applied electric field across the dielectric in MV/cm. The value must be voltage compensated for thin t_{ox} (otherwise the correction is insignificant) band bending if an accumulation layer is formed, but no compensation is needed if an inversion layer is formed. E_{ox} is the quotient of the compensated voltage & the oxide thickness, t_{ox}. Note that t_{ox} should be electrically or physically measured.

E_a = apparent activation energy, typically expressed in electronvolts (eV) = $(\Delta H)_o$

k = Boltzmann's constant

T = temperature in kelvins

Previous work **[5.1.20]** at very large electric field shows that γ has a 1 / T dependence, which affects TTF equivalently to an activation energy that decreases linearly with the electric field,

$$E_{aa} = (\Delta H)_o - a\, E_{ox} \quad \textbf{(5.1.2)}$$

where

E_{aa} = apparent activation energy, typically expressed in electronvolts (eV); E_{aa} may be nearly temperature independent if several types of disturbed bonding states are present in the dielectric and the reaction rates are mixed during high field and/or high temperature TDDB testing

$(\Delta H)_o$ = the enthalpy of activation for bond breakage in the absence of external electric field (~2.0 eV in **[5.1.12, 5.1.24, 5.1.25]**)

a = effective molecular dipole-moment for the breaking bonds (~7.2 eÅ and a-range is 7 to 13 eA in **[5.1.12, 5.1.24, 5.1.25]**)

5.1.2 Models (cont'd)

5.1.2.1 E model [5.13 to 5.1.16] (cont'd)

For intrinsic failures in SiO_2 dielectrics of thickness ~<10 nm, γ = ~2.5 to 3.5 Naperians per MV/cm (~1.1 to 1.5 decades per MV/cm) and E_{aa} = 0.6 to 0.9 eV. For extrinsic defects, effective oxide thickness can be quite thin, and therefore, the effective field can be very large, which may reduce temperature sensitivity.

Long-term TDDB studies **[5.1.17]** showed that TDDB data were described effectively by the E model **[5.1.13 to 5.1.16]** while TDDB data published in **[5.1.18]** followed the 1/E model **[5.1.19 to 5.1.23]**. All models are now based on fundamental, physical parameters (not empirically fitted parameters) and fit TDDB data quite well **[5.1.17, 5.1.24, 5.1.25]**. The key issue is whether any given model can also obey the Poisson area scaling, which is universally accepted.

The good fit of the physics-based E model to the low field/long-term TDDB data strongly suggests electric field is the dominant degradation driver at low stresses characteristic of customer applications and that constant current stress is NOT relevant to customer application.

5.1.2.1.1 TDDB numerical example using E model

Objective: Calculate the acceleration factor (AF) for gate oxide failure by TDDB for an office environment vs. a test structure accelerated environment.

Assumptions:
Office conditions are: 50 °C chip temperature (inside a desktop PC) & an electric field of 4 MV/cm
Accelerated condition (for a test structure) is: 300 °C & 8 MV/cm
effective molecular dipole-moment a: 7.2 eÅ
Field acceleration parameter, γ(50°C) : 2.586 Naperians (natural logarithm) per cm/MV
Field acceleration parameter, γ(300°C) : 1.4577 Naperians (natural logarithm) per cm/MV

Apparent activation energy, E_{aa}: 0.75 eV (approximate center of the nominal range for E_{aa})

AF, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = \exp[-(\gamma(T_{office})E_{office} - \gamma(T_{accel})E_{accel})] * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{accel})]$$

$$AF = \exp[-(2.586 \text{ cm/MV} * 4 \text{ MV/cm} - 1.4577 \text{ cm/MV} * 8 \text{ MV/cm})] * \exp[(0.75 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 50)\text{K} - 1 / (273 + 300)\text{K})]$$

$$AF = 3.7344 * 1.27 \times 10^{5} = 4.7462 \times 10^{5}$$

Conclusion: So, moving from the accelerated test structure environment to the office environment will increase TTF value to 2 x 10^{10} times the accelerated stress value, of which 160,000 X is due to electric field and 127,000 X is due to temperature. One must consider whether the same failure mechanisms are active under such a heavily accelerated stress vs ordinary operation.

NOTE Many papers in the literature may use and plot base 10 (rather than base e) when expressing the field acceleration factor. One should be careful to note whether base 10 or natural base e is being used. Some authors, for clarity reasons, will write the field acceleration as decades per MV/cm to emphasize that the base 10 is being used or Naperians per MV/cm to emphasize that the natural base e is being used. Many authors, however, may not emphasize this distinction to the reader, so the reader must be cautious. The conversion factor between base 10 and base e is 2.3:1, i.e., $\gamma_{base\ e} = 2.3 * \gamma_{base\ 10}$. In this document, the natural base e is assumed.

5.1.2 Models (cont'd)

5.1.2.2 1/E model [5.1.19 to 5.1.23]

The cause of TDDB (even at low fields) is postulated to be due to current through the dielectric by Fowler-Nordheim (F-N) conduction. F-N injected electrons (from the cathode) cause impact ionization damage of the dielectric due to as they accelerate through the dielectric. Additionally, when these accelerated electrons reach the anode, hot holes may be produced that can tunnel back into the dielectric causing damage (hot-hole anode injection mechanism). The time-to-failure is expected to show an exponential dependence on the inverse of electric field, $1 / E_{ox}$:

$$TTF = \tau_o(T) * \exp(G(T) / E_{ox}) \quad \textbf{(5.1.3)}$$

where

$\tau_o(T)$ = temperature dependent pre-factor (~1×10^{-11} s)
$G(T)$ = field acceleration parameter (~350 MV/cm with a weak temperature dependence)
E_{ox} = externally applied electric field across the dielectric in MV/cm. It must be voltage compensated for band bending if an accumulation layer is formed, but no compensation is needed if an inversion layer is formed. E_{ox} is the quotient of the compensated voltage & the oxide thickness, t_{ox}. Note that t_{ox} should be electrically or physically measured.

5.1.2.3 V model [5.1.26 to 5.1.27]

Two papers at 2000 IRPS reported data that showed the E model was no longer valid for gate oxide thickness values <4 nm. It was found that a model exponential with voltage rather than electric field represented the reliability performance well. Thus, the time-to-failure is expressed as:

$$TTF = A_o * \exp(-\beta V) * \exp(E_{aa} / kT) \quad \textbf{(5.1.4)}$$

where

A_o = arbitrary scale factor, dependent upon materials & process details
β = voltage acceleration parameter
V = applied voltage
E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)
k = Boltzmann's constant
T = temperature in kelvins

5.1.2.4 Power-law model [5.1.28 to 5.1.37]

In recent years for gate oxide thickness <2 nm, a power-law for voltage dependence of oxide breakdown is proposed based on extensive experimental database including long-term module stress **[5.1.28]**. Several research groups independently experimentally confirmed this model **[5.1.29 to 5.1.34]**. Work reported at 2006 IRPS demonstrates the power-law voltage dependence remains valid over twelve orders of magnitude from micro second time frames to hundred hours time span **[5.1.32]**.

The power-law model was originally proposed based on the experimental work on ultra-thin oxides below 5 nm **[5.1.28]**. Most importantly, the power-law model preserves important breakdown characteristics, namely Poisson random statistics and weakest link property, which are universally accepted **[5.1.28]**. This model can be extended to describe a large range of oxide thickness up to 10 nm and at stress voltages as large as 12 V **[5.1.35]**. This model is also consistent with the current-driven breakdown property as demonstrated by independent experimental evidence using substrate carrier injection technique **[5.1.36]**. The physical interpretation of power-law voltage dependence has also been advanced by several groups by comparing experimental data with the first-principle theory and STM experiments of hydrogen desorption phenomenon **[5.1.29, 5.1.30, 5.1.35 to 5.1.37]**.

5.1.2 Models (cont'd)

5.1.2.4 Power-law model [5.1.28 to 5.1.37] (cont'd)

The time-to-breakdown is expressed as:

$$t_{BD} = t_o * V^{-n} \quad \textbf{(5.1.5)}$$

where n is the power-law exponent and t_o is the prefactor.

The exponent of power-law, n, is found to be independent of oxide thickness or only weakly dependent of oxide thickness. On the other hand, temperature dependence of oxide breakdown is generally complicated by many factors **[5.1.29]**. First of all, the power-law exponent is found to depend on temperature. The physics of this temperature dependence of power-law exponent are not clear at this moment **[5.1.34]**. Secondly, temperature dependence of oxide breakdown is shown to follow a non-Arrhenius activation rather than conventionally accepted Arrhenius activation. This suggests that activation energy is temperature dependent **[5.1.14]**, analogous to the voltage dependence of local voltage acceleration factor. Both the temperature dependent exponent and non-Arrhenius activation give rise to a large variety of experimental observations commonly found on ultra-thin oxides and also provide a link to the experimental findings in thick oxides. In practice, for limited range of temperature applications, an Arrhenius temperature activation can be used as an approximate solution for the time-to-breakdown:

$$t_{BD} = t_o * \exp(E_{aa} / kT) \quad \textbf{(5.1.6)}$$

where

t_o = reference time at some reference temperature
E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)
k = Boltzmann's constant
T = temperature in kelvins

For a detailed and more complete discussion of power-law model for voltage and temperature dependence of oxide breakdown, the readers are referred to the reference **[5.1.31]**. Earlier relevant work is shown in citations **[5.1.1 to 5.1.12]**.

5.1.3 Example of Time-Dependent Dielectric Breakdown – gate oxide

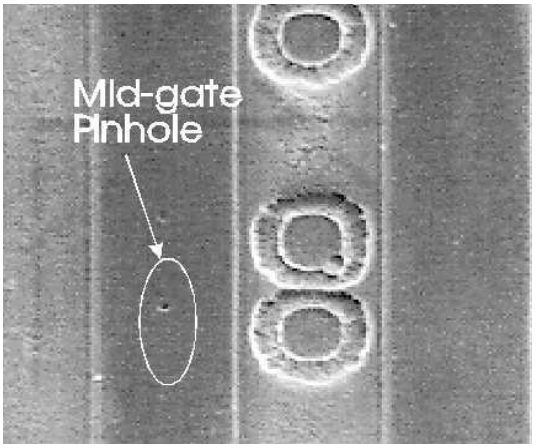


Figure 5.1-1 — Photograph of TDDB failure in a gate oxide — mid-gate

5.2 FEoL Failure Mechanisms – Hot Carrier Injection (HCI)

Hot carrier injection describes the phenomenon by which carriers gain sufficient energy to be injected into the gate oxide **[5.2.6 to 5.2.15]**. This occurs as carriers move along the channel in MOSFET and experience impact ionization near the drain end of the device. The damage can occur at the interface, within the oxide and/or within the sidewall spacer. Interface-state generation and charge trapping induced by this mechanism result in transistor parameter degradation, typically switching frequency degradation, rather than a "hard' functional failure.

5.2.1 Constraints and limitations

HCI-induced transistor degradation is well modeled by peak substrate current for the n-channels and peak gate current for the p-channels, at least for transistors at >0.25 μm. For sub-0.25 μm p-channel, the drive current tends to decrease like NMOS after hot carrier stress. For sub-0.25 μm p-channel, worst-case lifetime occurs at maximum substrate current stress. The time-to-failure (TTF) model is the same as n-channel. The drive currents for the n-channel transistors tend to decrease after HCI stressing; the p-channel drive current may increase/decrease depending on channel length and stress conditions. The off-state leakage can increase dramatically **[5.2.12]**, especially for initially high drive current p-channels.

There have been reports that the temperature dependence of substrate current has positive activation energy when V_{CC} is lower than 2.5 V **[5.2.1 to 5.2.3]**. The temperature dependent model for lower V_{CC} is still under investigation. A new energy driven paradigm is proposed for NMOSFET hot carrier effects. The driving force is the energy (voltage) instead of the electric field (lucky electron model) **[5.2.4]**. A gate-drain/source overlap asymmetry can result in worse hot carrier reliability **[5.2.5]**.

There is growing evidence that HCI physics may be starting to change at 0.25 μm and smaller, leading to changes in worst-case stress conditions **[5.2.4]**. Precise voltage models (rather than substrate current or gate current) would be very useful.

HCI evaluations are almost always performed on test structures rather than products and done under DC conditions, thus the calculated lifetime should be considered a figure of merit for process comparison. A short "lifetime" observed with DC test structures does NOT imply unacceptable product performance under AC conditions. For a digital circuit, like an inverter, HCI stress only occurs during the device turn-on and turn-off periods. These turn-on and turn-off periods are typically 1-2% of the overall cycle time. Hence, the conversion factor between DC stress and AC stress can be large. Note that this section treats device HCI when the transistor is conducting, but does not treat other effects when the device is not conducting (NBTI, PBTI, Drain-Gate stress, etc., which can have large duty cycle and different failure mechanisms).

Typically, HCI degradation causes reduced circuit speed rather than catastrophic failure; although, a large enough speed reduction can cause device failure. For products where the substrate or gate current is unknown, large voltage acceleration is possible because gate and substrate current are exponentially related to the reciprocal of the gate oxide electric field. HCI-induced transistor degradation modeling seems to be accurate, but the extrapolation from transistor degradation to circuit-level degradation is uncertain and should be the focus of future research efforts.

5.2 FEoL Failure Mechanisms – Hot Carrier Injection (HCI) (cont'd)

5.2.2 Models

Generally, degradation induced by the HCI can be described by:

$$\Delta p = A * t^n \quad \textbf{(5.2.1)}$$

where

- Δp = shift in device parameter of interest (V_T, g_m, I_{Dsat}, etc.)
- A = material dependent parameter
- t = stress time
- n = empirically determined exponent, a function of stress voltage, temperature, and effective transistor channel length

5.2.2.1 N-channel model

N-channel devices use an Eyring model. Eyring makes the practical assumption of mathematically separable, independent variables:

$$TTF = B * (I_{sub})^{-N} * \exp(E_{aa} / kT) \quad \textbf{(5.2.2)}$$

where

- B = arbitrary scale factor (strong function of proprietary factors such as doping profiles, sidewall spacing dimensions, etc.)
- I_{sub} = peak substrate current during stressing
- N = 2 to 4
- E_{aa} = apparent activation energy, -0.2 to +0.4 eV
- k = Boltzmann's constant
- T = temperature in kelvins

NOTE: The apparent activation energy can be negative or positive depending on channel length and voltage **[5.2.1 to 5.2.3]**.

5.2.2.2 P-channel model

5.2.2.2.1 For L >= 0.25 μm

$$TTF = B * (I_g)^{-M} * \exp(E_{aa} / kT) \quad \textbf{(5.2.3)}$$

where

- B = arbitrary scale factor (strong function of proprietary factors, such as doping profiles, sidewall spacing dimensions, etc.)
- I_G = peak gate current during stressing
- M = 2 to 4
- E_{aa} = apparent activation energy, -0.1 to -0.2 eV
- k = Boltzmann's constant
- T = temperature in kelvins

NOTE A rough "rule-of-thumb" for the gate current versus voltage dependence of p-channel devices is peak gate current doubles for each 0.5 V increase in drain-source voltage (V_{DS}).

5.2.2 Models (cont'd)

5.2.2.2 P-channel model (cont'd)

5.2.2.2.2 For L <0.25 μm

$$TTF = B * (I_{sub})^{-N} * \exp(E_{aa} / kT) \quad \textbf{(5.2.4)}$$

where

- B = arbitrary scale factor (strong function of proprietary factors such as doping profiles, sidewall spacing dimensions, etc.)
- I_{sub} = substrate current during stressing at $V_G = V_D$
- N = 2 to 4
- E_{aa} = apparent activation energy, +0.1 to +0.4 eV
- k = Boltzmann's constant
- T = temperature in kelvins

5.2.3 HCI numerical example

Objective: Calculate the acceleration factor (AF) for Hot Carrier Injection for an office environment vs. a test structure accelerated environment.

Assumptions:
Office conditions are: 50 °C chip temperature & substrate current of 1 μA
Accelerated conditions are: -40 °C & 10 μA substrate current
Substrate current is accelerated by elevating V_{CC}
N value of 3
Apparent activation energy, E_{aa}: -0.15 eV

AF, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = [(I_{sub,\,office} / I_{sub,\,accel})^{-N}] * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{accel})]$$

$$AF = [(1\ \mu A / 10\ \mu A)^{-3}] * \exp[(-0.15\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K - 1 / (273 - 40)K)]$$

$$AF = 1 \times 10^{3} * 8 = 8000$$

Conclusion: So, moving from the accelerated test structure environment to the office environment will increase TTF value to 8000 times the accelerated stress value, of which 1000 X is due to substrate current and 8-fold is due to temperature.

5.3 FEoL Failure Mechanisms – Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is a wearout mechanism experienced by PMOSFETs with the channel in inversion **[5.3.1 to 5.3.18]**. It is believed that NBTI is controlled by an electrochemical reaction where holes in the PMOSFET inverted channel interact with Si compounds (Si-H, Si-O, etc) at the Si/SiO_2 interface to produce donor type interface states and possibly positive fixed charge. NBTI damage is generated by cold holes (thermalized) in the inverted channel. Attention must be paid not to confuse this mechanism with PMOSFET damage generated by possible impact ionization at high V_G regime which produces hot hole damage. The relative contribution of the NBTI induced interface states generation and positive fixed charge formation is very sensitive to the gate oxide process used in the technology. The electrochemical reaction is strongly dependent on the gate oxide electric field (V_G / t_{ox}) and the channel temperature. The NBTI damage may lead to substantial PMOSFET parameter changes, in particular to an increase of the absolute value of the threshold voltage (transistor is harder to turn on) as well as mobility degradation with consequent reduction in drive current.

5.3.1 Constraints and limitations

NBTI is a limiting factor in scaling CMOS submicron technologies for the following main two reasons:

- NBTI has a strong dependence on the gate oxide process. Nitrided oxides are more sensitive to NBTI than thermal oxides. Nitrided oxides are needed in thinning the gate oxide to reduce Boron penetration.
- The vertical gate oxide electric field is observed to increase with CMOS scaling.

Recent work has shown relaxation effects after stopping the NBTI stress, resulting into a recovery of the NBTI damage which has two important effects:

- Typical testing of device parameters after the NBTI stress is somewhat sensitive to the NBTI recovery. The measured parameter shift strongly depends on the testing sequence and tester used
- Because of the fast recovery effects, it is expected that AC-level NBTI is less than what is measured in DC at the same voltage and temperature stress bias conditions. A general relation between DC and AC NBTI is not established yet. It is expected to be frequency independent, but duty cycle dependent

NBTI stresses are typically performed on test structures rather than products and under DC bias conditions. The estimated DC lifetime should be considered a figure of merit for a process or technology comparison. A short DC NBTI “lifetime” does not imply unacceptable product performance under AC conditions.

GIDL leakage (Gate-Induced-Drain-Leakage) can increase due to NBTI (especially as nitrided oxides are more sensitive to NBTI than pure Si oxides) as consequence of hole damage in the gate-drain overlap region, while the channel off current is reduced. Typically, NBTI degradation causes reduced circuit speed rather than catastrophic failure; although, clearly a large enough speed reduction can cause circuit failure. Circuits allowing large voltage overshoots may be more sensitive to NBTI given the large gate voltage acceleration of this mechanism.

A given PMOSFET in a circuit is exposed to the NBTI damage as long as it operates in inversion. For this reason NBTI is sensitive to stand-by conditions (‘0’ input on an inverter for example), contrary to Channel Hot Carrier, which is typically active during voltage transients.

Larger NBTI induced V_T mismatching is expected in small area PMOSFET transistors – this is particularly true for SRAM. This is the result of the larger broadening of device parameters observed after NBTI with PMOSFET area scaling.

5.3 FEoL Failure Mechanisms – Negative Bias Temperature Instability (NBTI) (cont'd)

5.3.1 Constraints and limitations (cont'd)

NBTI can be enhanced by BEoL charging. Circuit and device design need to be optimized to minimize this effect.

5.3.2 Models

The current state of the NBTI models is limited by the knowledge of the physics for this mechanism. For a given gate oxide thickness (t_{ox}), either one of the following phenomenological models is generally used to describe the NBTI degradation:

$$\Delta p = A_o * \exp(E_{aa} / kT) * (V_G)^{\alpha} * t^n \quad \textbf{(5.3.1)}$$

or

$$\Delta p = A_o * \exp(E_{aa} / kT) * \exp(\beta V_G) * t^n \quad \textbf{(5.3.2)}$$

where

- Δp = shift in device parameter of interest (V_T, $\%g_m$, $\%I_{Dsat}$, etc.)
- A_o = pre-factor dependent on the gate oxide process and CMOS technology
- E_{aa} = apparent activation energy (experimentally measured values range between -0.01 to +0.15 eV)
- k = Boltzmann's constant
- T = channel temperature in kelvins
- V_G = absolute value of the gate voltage applied to the PMOSFET device in inversion
- α = measured gate voltage exponent (measured values range between 3 to 4)
- β = measured gate voltage sensitivity, units are reciprocal of Voltage
- t = stress time
- n = measured time exponent (measured values range between 0.15 to 0.25)

Assuming **(5.3.1)** is applicable, the following time-to-failure (TTF), for a given accepted Δp failure criterion (Δp_t), is:

$$TTF = [\Delta p_t / A_o * \exp(E_{aa} / kT_{appl}) * (V_{G,\,appl})^{\alpha}]^{1/n} \quad \textbf{(5.3.3)}$$

where

- A_o = pre-factor dependent on the gate oxide process and CMOS technology
- E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)
- k = Boltzmann's constant
- T_{appl} = application channel temperature in kelvins
- $V_{G,\,appl}$ = application gate voltage
- α = measured gate voltage exponent
- n = measured time exponent

In the case where **(5.3.2)** is applicable, TTF becomes:

$$TTF = [\Delta p_t / A_o * \exp(E_{aa} / kT_{appl}) * \exp(\alpha V_{G,\,appl})]^{1/n} \quad \textbf{(5.3.4)}$$

where symbols in equation **(5.3.4)** have the same meanings as in **(5.3.3)**.

The failure criterion Δp_t is defined in terms of an allowed PMOSFET parameter shift such as ΔV_T or $\%I_{Dsat}$. Typically, the selection of a given failure criterion should depend on the circuit sensitivities and requirements of the PMOSFET device under investigation.

5.3 FEoL Failure Mechanisms – Negative Bias Temperature Instability (NBTI) (cont'd)

5.3.3 NBTI numerical example

Objective: Calculate the acceleration factor (AF) defined as the ratio between TTF for application conditions (TTF_{appl}) over TTF for accelerated conditions (TTF_{accel}), i.e., $AF = TTF_{appl} / TTF_{accel}$

Assumptions:
The application temperature and bias conditions are: 50 °C chip temperature & V_G = -1.0 V
The accelerated temperature and bias conditions are: 140 °C & V_G = -1.5 V
α value of 3.5
n value of 0.25
Apparent activation energy, E_{aa}: -0.02 eV

Using **(5.3.3)** we have:

$$AF = [(V_{G,\,accel} / V_{G,\,appl})^{\alpha / n}] * \exp[(E_{aa} / k)(1 / T_{accel} - 1 / T_{appl})(1 / n)]$$

$$AF = [(1.5\ V / 1\ V)^{3.5 / 0.25}] * \exp[(-0.02\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 140)K - 1 / (273 + 50)K)(1 / 0.25)]$$

$$AF = 292 * 1.87 = 546$$

Conclusion: So, moving from the accelerated stress conditions to the application conditions will increase TTF value to 546 times the accelerated stress value.

5.4 FEoL Failure Mechanisms – Surface inversion (mobile ions)

Alkaline-metal elements such as Li, Na, and K can sometimes be found in the semiconductor processing materials. In SiO_2, these ions are very mobile under the presence of modest electric fields (~0.5 MV/cm) and temperatures (100 °C). An accumulation of the drifted ions at the Si/SiO_2 interface can cause surface inversion and lead to increased leakage and device failure **[5.4.1 to 5.4.5]**.

Sodium and potassium are the usual mobile ion suspects, simply because of their high mobility and their relative abundance in many materials. Under bias, they can drift from the polysilicon anode to the silicon substrate (cathode). A build-up of positive ions at the Si/SiO_2 interface can invert the surface and severely degrade the oxide isolation. Ionic drift in the SiO_2 gate dielectric can also cause premature TDDB. In the case of EPROMs, mobile ion accumulation around the negatively-charged polysilicon floating-gate can lead to data retention fails.

Devices showing such inversion-induced leakage failures can recover during an unbiased high temperature bake. The bake causes a redistribution of the mobile ions away from the accumulated Si/SiO_2 interface (or polysilicon floating-gate in the case of an EPROM-like device).

5.4.1 Constraints and limitations

The activation energy for mobile ion diffusion depends on several factors:

- Diffusing species
- Medium through which the mobile ions diffuse
- The concentration of the contaminant

Generally, one finds activation energies for mobile ion diffusion in SiO_2 (and along its interfaces) in the 0.75 to 1.8 eV range **[5.4.1 to 5.4.7]**. Citation **[5.4.5]** calculates activation energy values from fundamental physical parameters for 25 different species (charge zero, +1 or +2) and is deemed the most reliable source, especially as its values are largely corroborated by later research.

5.4 FEoL Failure Mechanisms – Surface inversion (mobile ions) (cont'd)

5.4.2 Models

Mobile ions are influenced by both electric field and temperature. An Eyring model for time-to-failure can be written:

$$TTF = A * (< J_{ion} >)^{-1} * exp(E_{aa} / kT) \quad \textbf{(5.4.1)}$$

where

A	=	material dependent constant
$< J_{ion} >$	=	$< (e E \rho D_o / kT) – (D_o \partial\rho(x,t) / \partial x) >$ is the time-averaged mobile ion flux
E_{aa}	=	apparent activation energy for mobile ion diffusion (0.75 to 1.8 eV)
k	=	Boltzmann's constant
T	=	temperature in kelvins

The time-averaged mobile ion flux $< J_{ion} >$ has two components:

1. $(e E \rho D_o / kT)$ is the drift component which causes surface inversion during device operation, where:
   - e is the electronic charge on the mobile ion
   - E is the electric field across gate dielectric
   - ρ is the mobile ion density
   - D_o is the diffusion coefficient
2. $(D_o \partial\rho(x,t) / \partial x)$ is the back diffusion component (or recovery component).

For drift dominated failure (i.e., recovery component is small), the time-to-failure equation **(5.4.1)** reduces to:

$$TTF = A * (kT / e E \rho D_o) * exp(E_{aa} / kT) \quad \textbf{(5.4.2)}$$

5.4.3 Mobile ion numerical example

Objective: Calculate the acceleration factor (AF) for surface inversion between a use environment and an accelerated stress environment.

Assumptions:
The use temperature and bias conditions are: 50 °C chip temperature & V_G = 3.3 V
The accelerated stress temperature and bias conditions are: 150 °C & V_G = 5.0 V
Apparent activation energy, E_{aa}: 0.75 eV (Na+ drift dominated failure)

Using equation **(5.4.2)**, the acceleration factor (AF) becomes:

$$AF \text{ (ratio of } TTF_{use} \text{ to } TTF_{accel} \text{ values)} = (T_{use} / T_{accel})(V_{G,\,accel} / V_{G,\,use}) * \exp[(E_{aa} / k)(1 / T_{use} – 1 / T_{accel})]$$

$$AF = ((273 + 50)K / (273 + 150)K)(5.0\ V / 3.3\ V) * \exp[(0.75\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K – 1 / (273 + 150)K)]$$

$$AF = [0.7636 * 1.515]* 583.0 = \sim 675$$

Conclusion: The acceleration factor (from accelerated stress environment to the use environment) is ~675. Of this total acceleration factor, ~1.16 X is due to mobile ion flux while ~583 X is due to temperature.

5.5 FEoL Failure Mechanisms -- Floating-Gate Nonvolatile Memory Data Retention

Nonvolatile memories are subject to several mechanisms that can cause data to be lost. For floating-gate memories, a cell's data ('0' or '1') depends on whether its threshold voltage (V_T) is above or below a critical threshold level ($V_{T,crit}$). The threshold voltage may shift over time, leading to a change in data. The most common mechanisms for threshold drift are dielectric charge leakage and dielectric charge detrapping.

5.5.1 Constraints and limitations

These models apply to silicon floating-gate memories which are erased via tunneling through a 7 to 12 nm thick oxide or nitrided oxide. It is assumed that cell V_T is linear with stored charge, which is true for most common floating-gate memories. Devices such as split-gate memories with nonlinear responses require corrections to the equation terms which contain V_T. The models apply to the best-studied intrinsic data retention mechanisms but do not necessarily apply to other mechanisms.

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention

5.5.2.1 Mechanisms affecting data retention: classification, relevance, and mutual interaction

Several microscopic mechanisms contribute to data retention failure mechanisms, limiting the lifetime of Flash EEPROM devices and other similar non-volatile memories.The majority of these mechanisms are related to the presence of defects in the cell tunnel-oxide or IPD. Defects are mostly generated during cycling, causing degradation of the tunnel-oxide and trapping of charge therein. Charge can then be released both from the FG and from the tunnel-oxide, therefore causing V_T instabilities, both during post-cycling data retention periods and in the time lapses occurring in-between program/erase (P/E) cycles, giving rise to intermediate damage recovery **[5.5.5, 6]**.
The mechanisms having emerged as the main contributors to V_T instabilities in nowadays Flash technologies are:

- SILC, caused by trap-assisted tunneling (TAT), resulting in leakage of charge to/from cell FG **[5.5.1]**
- Interface states annealing, affecting cell V_T via enhancement of channel conductivity **[5.5.12, 13]**
- Charge detrapping, being originated by the capture of charge in oxide defects and by its subsequent neutralization **[5.5.14]**

Recent studies carried on at 2X-nm and 1X-nm NAND Flash nodes **[5.5.15-17]** reveal that the mechanisms can act simultaneosly, and that their relative weight on the overall V_T shift (ΔV_T) is not only dependent on the operating conditions of the device, i.e. temperature, programming level and cycling dose (N_{cyc}), but also on the technology being object of study. The measured ΔV_T transients reported in [5.**5.18, 19**], indeed, can be ascribed to charge detrapping alone, whereas those reported in [5.**5.15, 16]** (see Figure 5.5-1(a) for an example) display more complex behaviors and call for the inclusion of all the phenomena at the same time.

It should be also pointed out that the effects of the failure mechanisms cannot be simply superimposed in all operating conditions, i.e. the mechanisms are not independent. This is especially true when Flash cells are in the erased state (negative V_T), where both the tunnel-oxide field and the IPD field push detrapped electrons towards the FG. In this case, as shown in [5.**5.17]**, TAT is dominant at low N_{cyc}, while the large amount of detrapping taking place towards the FG at high N_{cyc} causes the FG to increase its energy level, therefore making TAT less likely because of the increased energy barrier.

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.2.1 Mechanisms affecting data retention: classification, relevance, and mutual interaction (cont'd)

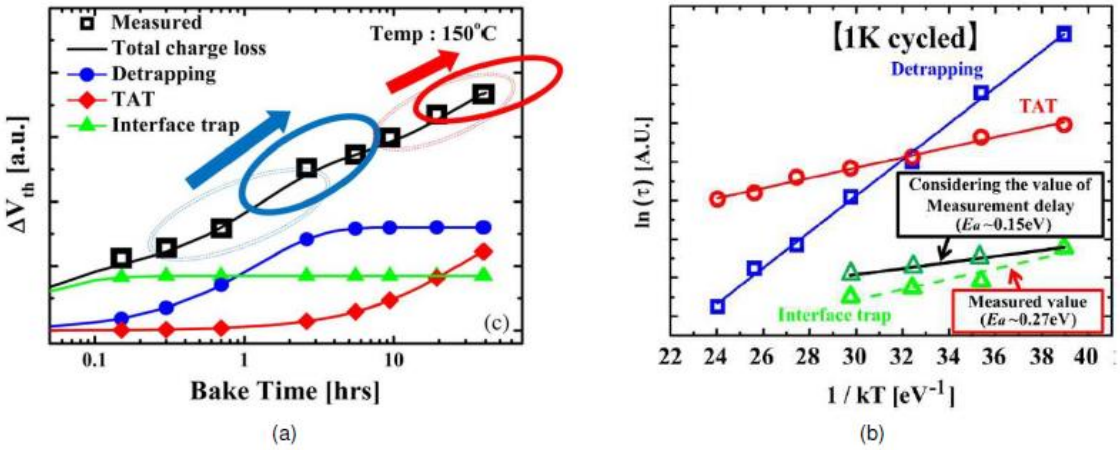


Figure 5.5-1 – (a) Example of failure mechanisms scenario affecting ΔV_T during data retention (from [5.5.16]), and (b) extraction of Eaa for each mechanism (from [5.5.15]).

5.5.2.2 Thermal activation

In order to accurately model and predict the behavior of Flash arrays for reliability analyses, not only the knowledge of the relative impact of the failure mechanisms on the overall retention ΔV_T is required, but also the assessment of their temperature dependence. In this way, accelerated retention tests can be designed, which are effective in predicting the on-field behavior of the device. The temperature dependence of charge detrapping, TAT and interface state annealing is simply reproduced by using an Arrhenius model. The apparent activation energy (E_{aa}) of each mechanism can be extracted, e.g., by using the compact model in [5.**5.16**].

Results, which have general validity, are shown in Figure 5.5-1(b). While the E_{aa} of charge detrapping is ~1.1 eV [5.**5.18**], TAT and interface states annealing have a weaker thermal activation, with E_{aa} values of 0.0-0.3 eV [5.**5.1, 5.5.15**] and ~0.15 eV [**5,7**], respectively. The time-to-temperature conversion law for each mechanism, allowing to convert a stress period t_{stress} spent at temperature T_{stress} to a use period t_{use} spent at temperature T_{use} is then:

$$t_{use} = t_{stress} \cdot \exp[(E_{aa}/k) * (1/T_{use} - 1/T_{stress})] \quad (\mathbf{5.5.1})$$

5.5.2.3 SILC-related dielectric leakage induced by program/erase cycling

High-field stressing of SiO_2 causes low field current leakage, called Stress-Induced Leakage Current or SILC. SILC is attributed to trap-assisted tunneling, whereby electrons or holes tunnel from one electrode to the other through traps generated by the stress. In memories, program/erase cycling causes the trap generation, and the resulting SILC causes V_T to drift. Programmed Flash cells may lose electrons (charge loss) and erased Flash cells may gain electrons (charge gain). The time-to-failure depends on cycle count, temperature, applied voltage, and the threshold voltage at which failure occurs **[5.5.1]:**

$$TF = A_o * (cycles^{-n}) * \exp[E_{aa}/kT] * \exp[-\gamma*(V_{T,Crit} - V_G)] \quad (\mathbf{5.5.2})$$

$$TF = A_o * (cycles^{-n}) * \exp[E_{aa}/kT] * \exp[-\gamma*(V_G - V_{T,Crit})] \quad (\mathbf{5.5.3})$$

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.2.3 SILC-related dielectric leakage induced by program/erase cycling (cont'd)

where equations **(5.5.2)** and **(5.5.3)** refer to charge-loss and charge-gain SILC, respectively, and where:

A_o = arbitrary scale factor, dependent upon materials & process details
cycles = number of program/erase cycles prior to the retention period
n = cycling power-law coefficient (typically 0.4 to 0.7)
E_{aa} = apparent activation energy (typically zero to 0.3 eV)
k = Boltzmann's constant
γ = field-acceleration coefficient, referenced to the V_T differential that creates the field in the oxide. Typically 2 to 6 V^{-1}.
$V_{T,crit}$ = cell threshold voltage at which the cell will be sensed as having incorrect data
V_G = applied voltage on the top or control gate of the cell during the retention stress. Zero for an unbiased stress (retention bake).

Temperature acceleration is usually avoided in SILC characterization, because E_{aa} is low and because high temperatures can cause the oxide to recover. Instead, electric-field acceleration is often used, using either margin testing (whereby devices are tested with a guardbanded value of $V_{T,crit}$) or an applied gate voltage (V_G).

The model formulae have been shown to accurately fit results taken over multiple years of retention time for some technologies. However, for other technologies there have been reports of deviations from a pure power-law dependence on cycle count and a pure exponential dependence on voltage **[5.5.2, 5.5.3].** In addition, it has been observed in some devices that threshold drift can abruptly stop when a certain threshold voltage is reached [5.**5.4**]. These effects are not comprehended by the model described above.

NOTE For given $V_{T,Crit}$ and V_G, the fraction of bits that are in error, called the bit error rate (BER), depends on the cycle count and the retention time. For BER<<1,

$$BER = BER_0 + B_o * (cycles^n * t^m) \quad (\mathbf{5.5.4})$$

where

BER_0 = BER at the beginning of the retention period, due to effects other than SILC
B_o = arbitrary scale factor, dependent upon materials and process details
t = retention time
m = retention-time power law coefficient, typically 1 to 2
n = power law exponent on number of program/erase cycles

In Flash memories designed to be used with error correction codes (ECC), the SILC-related leakage may cause some memory bits to fail even in an unaccelerated retention stress, though data loss does not occur since the BER does not reach the threshold at which the ECC capability is exceeded. In that case, an alternative method may be used: the BER may be measured as a function of time, fit to equation **(5.5.4)**, extrapolated to times beyond the stress time, and then compared to the ECC capability. The ECC capability can be calculated from the details of the ECC method used and the allowable failure rate, using equations that are well known in the field of ECC **[5.5.9**] but beyond the scope of this document. The capability calculated in this way is accurate only if the bit errors are randomly distributed, which is not perfectly the case in real devices. Accordingly, care must be taken to maintain a safety margin between the calculated ECC capability and the BER; this margin must be chosen to account for the variation of the BER from device to device and from one location of the device to another [5.**5.9**].

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.2.4 Charge detrapping

Generated traps directly affect the V_T of a cell when the traps are directly over the channel, and the V_T will shift if the traps detrap over time. Detrapping can occur under the influence of bias at room temperature or under the influence of elevated temperature. Acceleration results are available for elevated-temperature detrapping [NOR **5.5.5, 5.5.6**, NAND **5.5.7**].

Characterizing detrapping requires two reliability stresses in series – program/erase cycling followed by a data-retention bake. Detrapping in the bake, which can lead to data loss, depends not only on the time and temperature of the bake, but also on the time and temperature of the cycling period, because significant detrapping occurs during the delays between program/erase cycles. As a result, an accelerated reliability stress corresponds not to a single equivalent time under a chosen use condition, but to two such times, one for cycling and one for retention:

$$t_{cycling,use} = t_{cycling,stress} * \exp[(E_{aa}/k) * (1/T_{use} - 1/T_{cycling,stress})] \quad (\mathbf{5.5.5})$$

$$t_{retention,use} = t_{retention,stress} * \exp[(E_{aa}/k) * (1/T_{use} - 1/T_{retention,stress})] \quad (\mathbf{5.5.6})$$

where:

$t_{cycling,use}$	=	time over which cycling occurs at use condition
$t_{cycling,stress}$	=	time over which cycling is performed at accelerated stress condition
E_{aa}	=	apparent activation energy for detrapping (typically 1.1 to 1.2 eV)
k	=	Boltzmann's constant
T_{use}	=	temperature in kelvins at use condition
$T_{cyclin,stress}$	=	temperature in kelvins during cycling period at accelerated stress condition
$t_{retention,use}$	=	time over which retention period occurs at use condition
$t_{retention,stress}$	=	time over which retention period is performed at accelerated stress
$T_{retention,stress}$	=	temperature in kelvins during retention period at accelerated stress condition

5.5.2.4.1 Charge detrapping: statistical modeling

Models in [5.**5.16**] and [5.**5.18**] for charge detrapping are very simple and easy-to-use. These models are especially good when dealing with uniform cycling, where P/E cycles are done at a constant pace and cycling temperature is uniform throughout the cycling phase. The semi-analytic model described in [5.**5.19-21**], on the other hand, keeps into account the full trapping/detrapping dynamics during cycling and bake, therefore reproducing the effect of intermediate recovery in-between cycles (distributed-cycling effect) on the post-cycling data retention. As opposed to [5.**5.16**], where a single deterministic time constant is used for the detrapping mechanism, a whole spectrum of time constants is allowed, and is calculated according to the cycling experiment. In this way, any arrangement of cycles and delays can be emulated, with the delays having arbitrary lengths and temperatures. Also, the full ΔV_T distribution at generic retention time t_R can be calculated, whereas models in [5.**5.16**] and [5.**5.18**] only reproduce the average ΔV_T ($\langle \Delta V_T \rangle$). It should be noted that the model in [5.**5.19-21**] adds small complexity with respect to previous approaches, keeping the number of fitting parameters low.

The direct observation of single-electron detrapping events in cycled Flash arrays has highlighted that the main variability sources affecting charge loss are:

- the amount of V_T shift, ΔV_T[1], corresponding to each detrapping event
- the number of trapped (N) and detrapped (N_d) charges, with the latter being dependent on t_R
- the time, t_d, at which detrapping events take place, resulting from an exponential distribution with time constant τ_d

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.2.4.1 Charge detrapping: statistical modeling (cont'd)

The detrapping process is then modeled making reasonable assumptions on these variability sources. The spread in ΔV_T[1], due to percolative channel conduction, is reproduced via a suitable distribution. N, on the other hand, is assumed to be Poisson distributed among the cells. As a consequence, $N_d(t_R)$ is also Poisson distributed, with mean value, $\langle N_d(t_R)\rangle$, increasing with t_R. Finally, the detrapping time constant, t_d, is assumed widely spread over the logarithmic time axis. This choice is motivated by the observation that detrapping proceeds with t_R at a logarithmic pace.
A convenient mathematical tool, allowing to describe the distribution of trapped charges over time and its evolution during cycling/bake is the *average spectral density* of trapped electrons, $\langle n_d(\tau_d)\rangle$, allowing to quantify the amount of detrapping up to time t_R via

$$\langle N_d(t_R)\rangle = \int [\, \langle n_d(\tau_d)\rangle - \langle n_d(\tau_d)\rangle * \exp(-t_R/\tau_d)\,]\, d\log_{10}(\tau_d) \qquad (\mathbf{5.5.7})$$

i.e. by integrating the difference of the electron density at time t_R and prior to data retention. Here, the exponential term $\exp(-t_R/\tau_d)$ is the probability of emitting a charge within t_R, and, as t_R elapses, it yields a *detrapping front* (see Figure 5.5-2), gradually emptying the electron density along the time axis.

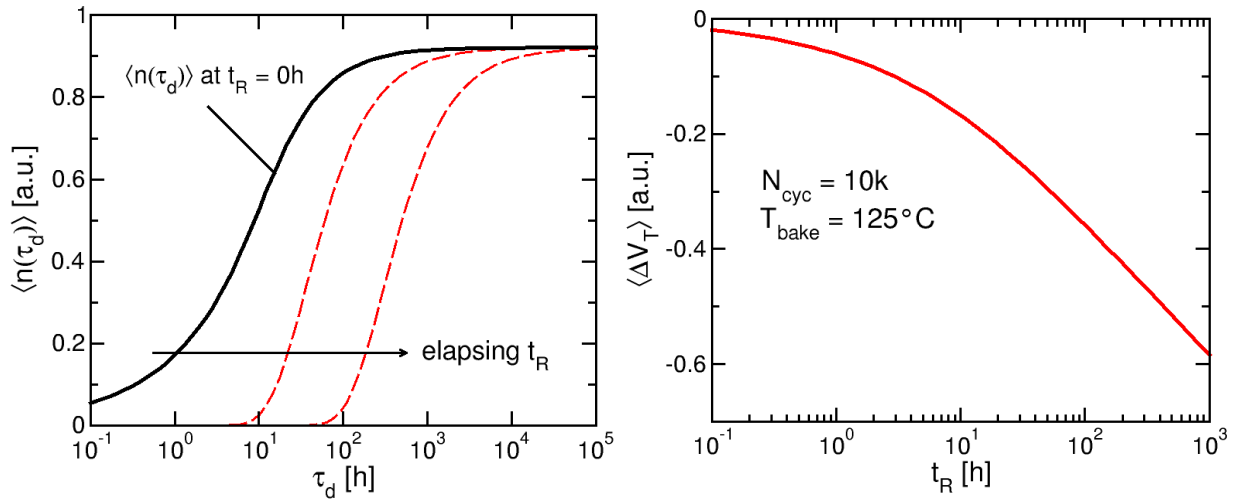


Figure 5.5-2 – (a) Spectrum of detrapping time constants immediatly after cycling (black curve) and during data retention (red curves), and (b) Resulting $\langle \Delta V_T(t_R)\rangle$ transient.

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.2.4.1 Charge detrapping: statistical modeling (cont'd)

The important observation here is that $\langle n_d(\tau_d)\rangle$ is dynamical, evolving both during cycling and during bake. In particular:

- The effect of one cycle is modeled as an increment $\langle \Delta n_d(\tau_d)\rangle$, tailored in such a way that the trapped charge increases based on the amount of charge already present at time τ_d, and that trapping is proportional to SQRT(N_{cyc}).
- The effect of a delay period t_{delay}, whether it takes place during cycling or during bake, is reproduced by multiplying $\langle n_d(\tau_d)\rangle$ by $\exp(-t_{delay}/\tau_d)$.

Once $\langle N_d(t_R)\rangle$ is known, the whole ΔV_T statistics at time t_R can be calculated. The average value and the variance of ΔV_T are:

$$\langle \Delta V_T(t_R)\rangle = - \langle N_d(t_R)\rangle * \langle \Delta V_T^1\rangle \quad (\mathbf{5.5.8})$$

$$\sigma^2_{\Delta VT}(t_R) = - \langle \Delta V_T(t_R)\rangle * (\langle \Delta V_T^1\rangle + \sigma^2_{\Delta VT1} / \langle \Delta V_T^1\rangle) \quad (\mathbf{5.5.9})$$

being $\langle \Delta V_T^1\rangle$ and $\sigma^2_{\Delta VT1}$ the average value and the variance of ΔV_T^1.

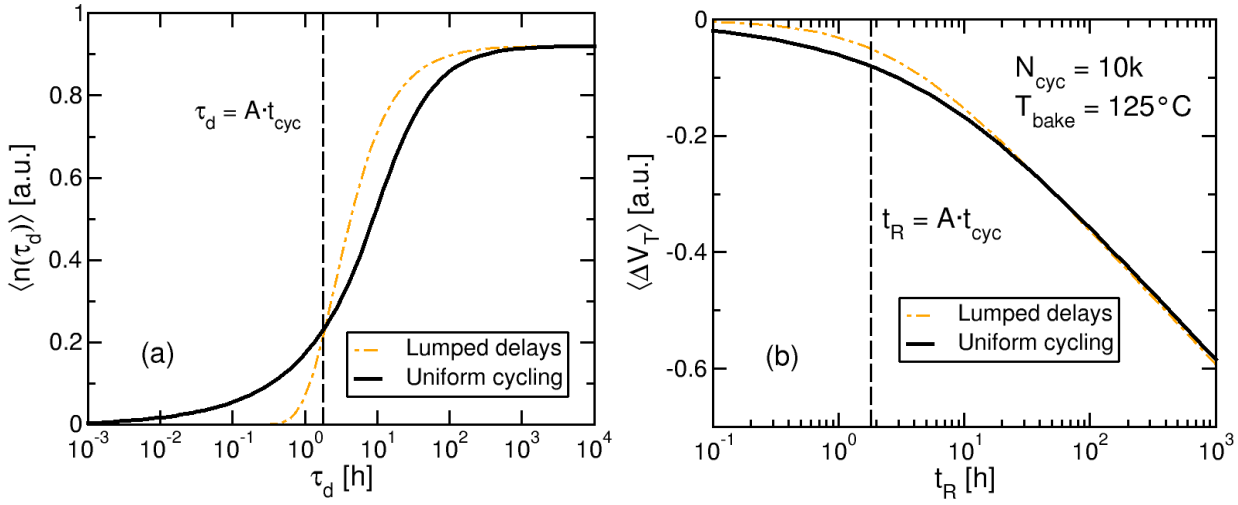
Whenever uniform cycling experiments are considered, having duration t_{cyc}, the described model agrees well with the empirical law [5.**5.18**]:

$$\langle \Delta V_T(t_R)\rangle = - \alpha * \log(1 + t_R / t_0) \quad (\mathbf{5.5.10})$$

which turns out to be exact in the case of a constant spectral density of trapped electrons.
Parameter α, i.e. the long-term slope of the $\langle \Delta V_T (t_R)\rangle$ transient, is proportional to $\langle n_d(\tau_d >> t_0)\rangle$ and to $\langle \Delta V_T^1\rangle$, being therefore strictly linked to the amount of trapped charge and to cell electrostatics.
The model allows gaining insight also on time t_0.
As an example of model use, let's investigate the spectral equivalent distribution between two cycling conditions. As shown in Figure 5.5-3, similar ΔV_T statistics are obtained when considering uniform cycling and a cycling experiment where $\langle n_d(\tau_d)\rangle$ is constant and all the delays between cycles are lumped in a single delay t_0 inserted prior to the bake. The delay, however, has not be of length t_{cyc}, but rather a fraction, $A \cdot t_{cyc}$, of the total cycling time. The reason is that, in uniform cycling, cycles done towards the end of the experiment have little time to recover, unlike cycles done in the beginning. The total lumped recovery time in the equivalent scheme is therefore less than the total cycling time. Analytical results show that A = 0.2 yields a good approximation.

5.5.2 Models for Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.2.4.1 Charge detrapping: statistical modeling (cont'd)



(a) **(b)**

Figure 5.5-3 – (a) Comparison of time constant spectra between uniform cycling of duration t_{cyc} and an equivalent cycling where all the delays are lumped in a single wait of duration $A \cdot t_{cyc}$ prior to the bake phase, and (b) Resulting $\langle \Delta V_T(t_R) \rangle$ transients. A = 0.2 results in similar V_T loss during data retention.

5.5.3 Data retention numerical example

Objective: Calculate the Acceleration Factors for data retention failure for an office environment vs an accelerated environment for both the detrapping and SILC mechanisms. For detrapping, also calculate the cycling stress conditions necessary to match the office environment after acceleration is considered. For SILC, use the voltage-acceleration method to calculate the acceleration factor. Separately, for SILC calculate the retention time-to-fail using the extrapolated-BER method.

Assumptions:

Use conditions are: 50 °C chip temperature (~T_{use}), with 100,000 cycles over a 2-year period (~$t_{cycling,use}$) followed by a retention period.

SILC accelerated stress conditions are: 100,000 cycles followed by a 25 °C retention period. For the voltage-acceleration method, margin testing will be used to guardband the failure level $V_{T,crit}$ by 2V. For the BER-extrapolation method, it will be assumed that the ECC scheme has a BER capability of 4E-5, that a factor-of-two margin of safety is desired based on an analysis of the BER nonuniformity, and that unaccelerated 1000-hour retention results are available with measurement points at 48, 168, 500, and 1000 hours.

Detrapping accelerated stress conditions are: 100,000 cycles performed at 85 °C, followed by a retention period at 125 °C.

5.5 FEoL Failure Mechanisms -- Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.3 Data retention numerical example (cont'd)

For SILC, $\gamma = 2.3\ V^{-1}$ and $E_{aa} = 0$ eV; and for detrapping, $E_{aa} = 1.1$ eV

For detrapping, the required cycling time in the accelerated stress is:

$t_{cycling,stress} = t_{cycling,use} * \exp[(-E_{aa}/k)*(1/T_{use} - 1/T_{cycling,stress})]$
$t_{cycling,stress} = 2 \text{ years} * \exp[(-1.1 \text{ eV} / 8.62x10^{-5} \text{ eV/K}) * (1/(273 + 50)K - 1/(273+85)K)]$
$t_{cycling,stress} = 2 \text{ years} * 0.0210 = 15 \text{ days}$

The AF for detrapping in bake is then:

$AF = t_{retention,use}/t_{retention,stress}$
$AF = \exp[(E_{aa}/k)*(1/T_{use} - 1/T_{retention,stress})]$
$AF = \exp[(1.1 \text{ eV} / 8.62x10^{-5} \text{ eV/K}) * (1/(273+50)K - 1/(273+125)K] = 1711$

For SILC using the voltage-acceleration method, the ratio of the TF values will be:

AF (ratio of TF values, office/accelerated) $= \exp[\gamma*(V_{T,crit,accel} - V_{T,crit,office})]$
$AF = \exp[(2.3\ V^{-1})*(2\ V)] = 99$

For SILC using the BER-extrapolation method, the following BER data points will be assumed:

Retention Time (Hours)	BER
0	0
48	5.63E-08
168	2.23E-07
500	7.41E-07
1000	1.59E-06

These data points would be extrapolated in time as shown below. In this example, the data fit a pure power-law relationship with zero for the BER_0 term. The ECC capability of $4x10^{-5}$ is divided by two to create the specified safety margin, as shown by the horizontal dashed line. The extrapolated BER line intercepts this horizontal dashed line at 10,000 hours, which would be the estimated retention time.

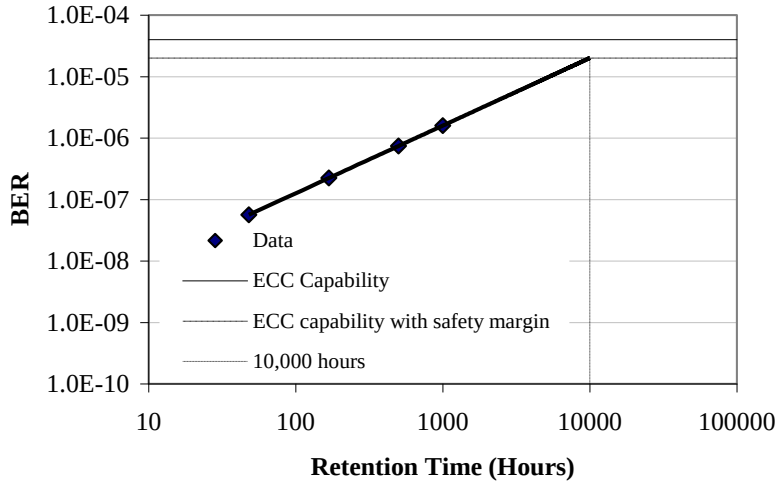


Figure 5.5-4 – Extrapolation of SILC bit error rate

5.5 FEoL Failure Mechanisms -- Floating-Gate Nonvolatile Memory Data Retention (cont'd)

5.5.3 Data retention numerical example (cont'd)

Conclusion: For detrapping, a choice of 15 days at 85 °C for the cycling condition causes the cycling conditions to match the office conditions, and then choosing 125 °C for the retention bake provides an acceleration factor of 1711. For SILC retention, a 2 V margin guardband provides an acceleration factor of 99 compared to the office environment. For SILC retention evaluated with the BER-acceleration method, the example data extrapolate to a TTF of 10,000 hours.

5.6 FEoL Failure Mechanisms – Localized Charge Trapping Nonvolatile Memory Data Retention

In localized charge-trapping NVM devices, such as NROM (Nitride Read Only Memory) devices, the threshold voltage of a cell (V_T) is determined by the quantity and the spatial distribution of the charge trapped locally in an ONO (Oxide-Nitride-Oxide) dielectric layer over the junction edge of an n-channel MOSFET transistor. Charges in NROM cells can be stored locally at both edges of each transistor, thus two physically separated bits can be stored in each cell **[5.6.1]**.

The reliability of data retention of NROM cells depends on the ability of the ONO layer to retain trapped charge. The primary data retention reliability detractor of NROM devices is migration of trapped charges, which may affect the threshold voltage of the cell. Lateral charge migration may occur due to thermally activated charge detrapping. NROM technology with bottom oxide thicker than 4 nm is relatively immune to vertical charge loss. Point defects in the bottom dielectric layer (SILC-type leakage) may cause the loss of only negligible fraction of the stored charge, because only charges trapped directly over the percolation path will be lost **[5.6.2]**.

5.6.1 Constraints and limitations

The model below applies to devices programmed by channel-hot-electron injection and erased by channel-hot-hole assisted tunneling **[5.6.7]**. Charge is injected from the n-channel of the transistor into a nitride layer of an ONO structure through 3 nm to 6 nm thick bottom oxide layer. The charge is stored locally near the junction edges.

The model considers the degradation of an unbiased NVM product as a function of time, temperature and number of endured program/erase cycles **[5.6.3]**. The model applies to cycled cells in which both types of charge carriers had been injected. Injection conditions and microscopic scattering mechanisms are different for holes and electrons, so the spatial distributions of trapped holes and trapped electrons in the dielectric layer are expected to be slightly different, resulting in an internal lateral dipole (multipole) **[5.6.4]**.

The relaxation of a dipole in disordered glasses is controlled by dispersive transport mechanism, resulting in a stretched exponential decay function **[5.6.5]**.

The model describes the decrease of V_T of a programmed cell from its high V_T state. Increase of V_T of the erased state over time (charge-gain) may also degrade the window of operation of NROM cell. The later mechanism and methods to suppress it are discussed elsewhere **[5.6.6]**.

5.6.2 Model

The decrease of V_T of programmed NROM cells is attributed to the migration of holes accumulated during cycling at the junction edges of the device. During long-term storage or under bake conditions at elevated temperatures these holes detrap and migrate laterally toward the electrons trapped further away over the channel, quenching their electric field and reducing the V_T of the cell. Electrons in the nitride are relatively immobile and hardly participate in the charge migration process.

5.6 FEoL Failure Mechanisms – Localized Charge Trapping Nonvolatile Memory Data Retention (cont'd)

5.6.2 Model (cont'd)

The kinetics of lateral migration of holes in the disordered nitride film follows dispersive transport mechanism **[5.6.2, 5.6.3]**. This mechanism involves multiple trapping and detrapping via a series of

events with stochastically increasing release times as the carriers fall from one trap to the next. It leads to a time-dependent diffusion coefficient and a stretched exponential kinetic behavior **[5.6.2]**. The change of V_T with time relative to its initial programmed state, ΔV_T, is described by:

$$\Delta V_T = \Delta V_{Tsat} * \{1 - \exp[-(t / \tau)^{\beta}]\} \quad \textbf{(5.6.1)}$$

$$\tau = \tau_o * \exp(E_\tau / kT) \quad \textbf{(5.6.2)}$$

$$\beta = T / T_o \quad \textbf{(5.6.3)}$$

where ΔV_{Tsat} is the saturation value of the retention degradation, t is storage time, T is storage temperature in kelvins, τ is a time constant, E_τ is a characteristic energy of the dipole relaxation process, k is Boltzmann's constant and τ_o and T_o are empirical coefficients. The parameters ΔV_{Tsat}, τ_o, and E_τ are product, process and cycle-count dependent **[5.6.2, 5.6.3]**. The value of the coefficient T_o was found to be 2550±100K for all NROM products tested to date, irrespective of Fab or technology node.

The Apparent Activation Energy **[5.6.3]** varies with number of cycles according to:

$$E_\tau = 0.75 + 0.07 * \log(\#\ \text{program/erase cycles});\ \text{in units of electronvolts (eV)} \quad \textbf{(5.6.4)}$$

A distinctive feature of NROM devices is that its retention loss saturates at a V_T level that is well above the neutral state of the cell. The magnitude of the saturation value ΔV_{Tsat} is cycle-count dependent. Saturation results from stopping of lateral migration, either because the limited quantity of excess holes available for migration had recombined with electrons, or because steady-state has been reached. The remaining electrons above the channel, after hole migration had stopped, determine the residual V_T after bake.

Let us denote by $\Delta V_{T\text{-}PR}$ the difference between the threshold voltage of the lowest bit in an ensemble of as-programmed bits (typically called the Program Verify level) and the threshold voltage of the critical reference Read level. $\Delta V_{T\text{-}PR}$ is a product dial-in parameter. The time for V_T to decrease by the amount $\Delta V_{T\text{-}PR}$ is the time-to-failure (TTF). From equation **(5.6.1)**, it can be shown that TTF is:

$$TTF = \tau * [-\ln(1 - \Delta V_{T\text{-}PR} / \Delta V_{Tsat})]^{1/\beta} \quad \textbf{(5.6.5)}$$

The cycle-count dependence of TTF enters via the power dependence of ΔV_{Tsat} on cycle-count **[5.6.2]**, and the temperature dependence of TTF enters via the temperature dependence of the parameters τ and β **[5.6.2, 5.6.3]**.

The thermal acceleration factor of the retention loss is obtained by dividing the time-to-failure at use conditions by the time-to-failure at high temperature stress:

$$AF = TTF_{use} / TTF_{stress} = \ldots \quad \textbf{(5.6.6)}$$

$$\exp[(E_\tau / k)(1 / T_{use} - 1 / T_{stress})] * [-\ln(1 - \Delta V_{T\text{-}PR} / \Delta V_{Tsat})]^{(1 / \beta use - 1 / \beta stress)}$$

If the dial-in parameter $\Delta V_{T\text{-}PR}$ is selected such that $\Delta V_{T\text{-}PR} / \Delta V_{Tsat}$ is equal to $1 - 1 / e = 0.632$, then the expression to the right of asterisk (*) in equation **(5.6.6)** equals 1 and equation **(5.6.6)** becomes identical to equation **(5.5.4)**.

5.6 FEoL Failure Mechanisms – Localized Charge Trapping Nonvolatile Memory Data Retention (cont'd)

5.6.3 Acceleration of cycling delays

Detrapping of holes between program/erase cycles results in relaxation of excess charge accumulated during cycling which in turn reduces the degradation during retention bake. Generally, in qualification experiments, the cycling rate is much faster than under use conditions. Consequently bake delays should be introduced during or between cycles, according to standards JESD22-A117A and JESD47E.

However, unlike equations **(5.5.3)** and **(5.5.4)** used in floating-gate technology, which use the same activation energy E_{aa} for cycling bake and for retention bake, in NROM devices the apparent activation

energy E_{aa} for cycling is generally smaller than the apparent activation energy for retention bake. That is because the parameter β in equation **(5.6.3)** is temperature dependent. Consequently $V_T(t)$ curves for different temperatures are not parallel and the space between them increases with time. Since the time duration between cycles is generally much shorter than the time duration of retention life (few hours vs. few years), the apparent activation energy E_{aa} for cycling is smaller than the apparent activation energy for retention bake.

5.6.4 Data retention numerical example

Objective: Calculate the acceleration factor (AF) and the stress time required to qualify a product for 5-year data retention at 50 °C after 100,000 cycles.

Assumptions:

Office conditions are: 50 °C chip temperature
Accelerated stress qualification conditions are: 125 °C
Activation energy, E_τ: 1.1 eV after 100,000 cycles **[5.6.3]**.

Let us assume that for the specific process and product dial-in selections, ΔV_{Tsat} (100,000 cycles) = 1.6 V, and the product was designed with program margins of $\Delta V_{T\text{-}PR}$ = 1.0 V.

From equation **(5.6.6)** we obtain:

$$AF = \exp[(E_\tau / k)(1 / T_{use} - 1 / T_{stress})] * [-\ln(1 - \Delta V_{T\text{-}PR} / \Delta V_{Tsat})]^{(1 / \beta use - 1 / \beta stress)}$$

$$AF = \exp[(1.1\text{ eV} / 8.62 \times 10^{-5}\text{ eV/K})(1 / (273 + 50)\text{K} - 1 / (273 + 125)\text{K})] * [-\ln(1 - 1\text{ V} / 1.6\text{ V})]^{(1 / \beta use - 1 / \beta stress)}$$

$$AF = \exp[(1.1\text{ eV} / 8.62 \times 10^{-5}\text{ eV/K})(1 / (273 + 50)\text{K} - 1 / (273 + 125)\text{K})] * \sim 1 = 1711$$

Also, from equation **(5.6.6)**:

$$TTF_{stress} = TTF_{use} / AF$$

$$TTF_{stress} = 5\text{ years} / 1711 = 25.6\text{ hours}$$

Conclusion: To qualify the product for 5-year data retention in office environment after 100,000 program/erase cycles, the product must withstand bake after cycling of 25.6 hours at 125 °C.

5.7 FEoL Failure Mechanisms – Phase Change (PCM) Nonvolatile Memory Data Retention

Phase Change Memories (PCM) store data by the resistance change of a thin-film chalcogenide material such as Germanium Antimony Tellurium (GeSbTe), with the most common compositional ratio being $Ge_2Sb_2Te_5$ (GST). However, many other phase change alloys and/or doping of these alloys have been proposed for electronic memory operation. The distinguishing aspect of PCM is that the resistance change of the thin film layer is associated with a thermally-induced phase change between crystalline and amorphous states of the material. The amorphous phase has a high resistivity and the crystalline phase has a significantly lower resistivity. In PCM the thermal stimulus is provided by an electrical pulse applied between two electrodes that are in direct contact with the phase change material located between them. The shape and amplitude of the electrical pulse determines whether the phase change layer is switched to amorphous or crystalline. The state of the memory is then accessed by measuring its resistance under a low electric field **[5.7.1-5.7.4]**.

In PCM, there are several mechanisms by which data could be lost. When utilized as a single-bit-per-cell (SBC), the cell is either in the 'SET' or 'RESET' state. Here the crystalline (low resistance) SET state is thermodynamically stable. However, the high resistance amorphous phase has two independent resistance-changing mechanisms: crystallization and resistance drift **[5.7.4]**. The drift process is a steady increase in the resistivity of the amorphous phase related to structural rearrangement of the chalcogenide and the dynamics of intrinsic traps **[5.7.5]**. Since the drift process increases the resistance of the high resistance amorphous state, it does not cause any data-loss for SBC PCM devices **[5.7.4]**. Data retention for a SBC PCM device is therefore determined by the cell's ability to retain the high resistance RESET state by avoiding undesired recrystallization of the amorphous material **[5.7.6]**.

5.7.1 Constraints and limitations

This model applies to phase change memories used for SBC operation. It is anticipated that PCM will eventually be utilized for storing multiple bits per cell (MBC). This will introduce more complexity in determining an accelerating factor for data retention and will be dependent on the specific details of how the MBC and reference bits are implemented in the design, and is outside the scope of this initial model **[5.7.7]**. In addition, it only considers data retention failures through crystallization, an intrinsic property of PCM materials, and cannot be generically applied to all defect mechanisms that may be encountered.

5.7.2 Models

5.7.2.1 Data retention failure due to crystallization of the amorphous reset state

As previously stated, the crystalline phase of PCM is thermodynamically stable. With time and temperature, the amorphous state will transition into this state via nucleation and growth of crystals in the solid amorphous phase **[5.7.6, 5.7.8]**. For proper operation as a nonvolatile memory, the crystallization time of the amorphous state must be sufficiently high to guarantee data retention over the duration and use conditions of the memory device. Crystallization of the $Ge_2Sb_2Te_5$ phase change alloy utilized in PCM is thermally activated and follows an Arrhenius law **[5.7.6, 5.7.8- 5.7.10]**. Crystallization times at use temperatures are years **[5.7.1-5.7.4, 5.7.10]**; therefore, accelerated experiments at high temperatures are required for an efficient evaluation of the crystallization properties of the active material **[5.7.1, 5.7.2, 5.7.6, 5.7.8, 5.7.9]**.

5.7.2 Models (cont'd)

5.7.2.1 Data retention failure due crystallization of the amorphous reset state (cont'd)

In PCM, data retention failures are realized when a cell initially programmed into the high resistance reset state is, on a subsequent read operation, found to be in the set state. This occurs when the resistance drops below a fixed value R_{FAIL} depending on the sensing algorithm in the memory array. The time necessary for the resistance to drop below R_{FAIL} is referred to as the time to failure, TTF. For relatively low temperatures (< 200 °C) both nucleation and growth mechanisms are controlled by the atomic diffusion barrier and crystallization kinetics that can be approximated by an Arrhenius law **[5.7.6, 5.7.8, 5.7.10-5.7.14]**. This is given by:

$$TTF = A_o * \exp(E_{aa} / kT) \quad \textbf{(5.7.1)}$$

where equation **(5.7.1)** refers to:

A_o = arbitrary scale factor, dependent upon materials & process details
E_{aa} = apparent activation energy for GST retention failure (typically 2.5eV)
k = Boltzmann's constant
T = temperature in kelvins
TTF = Time To Failure

The thermal acceleration factor of the retention loss is obtained by dividing the time-to-failure at use conditions by the time-to-failure at high temperature stress:

$$AF = TTF_{use} / TTF_{stress} = \exp[(E_{aa} / k)(1 / T_{use} – 1 / T_{stress})] \quad \textbf{(5.7.2)}$$

JEDEC Standard JESD91A, Method for Developing Acceleration Models for Electronic Component Failure Mechanisms, provides a reference procedure for extracting E_{aa} from a measured 50% fail point (t_{50}) at multiple temperatures. In addition, the following characteristics of PCM should be considered when developing acceleration models for PCM.

First, in test structures or specially designed characterization arrays the PCM resistance is frequently monitored at the bake temperature to permit greater acceleration. In this case, the combination of amorphous resistivity dependence on temperature and the drift phenomena can change the effective threshold fail resistance (R_{Fail}) and lead to errors in the calculated E_{aa} **[5.7.8]**. Reliable extraction of the E_{aa} should be obtained by taking multiple measurements at longer times (lower bake temperatures) and cooling the array down to perform all resistance measurements at a fixed temperature **[5.7.8]**.

Second, a widely accepted physical model for intrinsic data retention loss in PCM is a percolation-like conduction through the resulting mixed-phase structure **[5.7.9]**. Experimental results that consider repeated retention measurements on the same device result in varying retention times, thus demonstrating the stochastic component to GST crystallization. As a consequence, PCM data loss is expected to have a stochastic behavior, and a statistical analysis for the resistance-loss evolution is required **[5.7.9]**. Failure times driven by percolation dynamics typically obey Weibull statistics **[5.7.6, 5.7.9, 5.7.12]**. When considering the distribution of failure times of an array of cells, this can fit either a Weibull or a log-normal distribution **[5.7.10]**. When extracting the E_{aa}, sufficient sampling of retention fails is required to address this statistical nature of the retention times.

Finally, data to date on the PCM alloy $Ge_2Sb_2Te_5$ shows that cycling has a relatively small impact on retention (in some cases actually improving the data retention.) However, this behavior may be dependent on the particular PCM alloy or technology implementation. As a result, data retention and acceleration model analysis should be performed both prior to and post-cycling as part of the qualification procedure **[5.7.10]**.

5.7 FEoL Failure Mechanisms – Phase Change (PCM) Nonvolatile Memory Data Retention (cont'd)

5.7.3 Data retention numerical examples

Objective: Calculate the acceleration factor for data retention failure in an office environment vs. an accelerated environment. Perform one calculation for a stress designed to accelerate PCM data retention fails due to crystallization of the amorphous reset state.

Assumptions:
User conditions are: 55 °C chip temperature (~T_{use}). For $Ge_2Sb_2Te_5$ it is assumed that E_{aa} = 2.5 eV.

The AF for PCM data retention in a 85 °C bake is then:

$$AF = t_{retention,\ use} / t_{retention,\ stress}$$

$$AF = \exp[(E_{aa} / k)(1 / T_{use} - 1 / T_{retention,\ stress})]$$

$$AF = \exp[(2.5\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 55)K - 1 / (273 + 85)K)] = 1637$$

Conclusion: For PCM data retention a choice of 100 hr bake at 85 °C will be equivalent to 163,700 hours (18.7 years) at a use condition of 55 °C

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) ILD/Low-k/Mobile Cu ion

5.8.1 Low-k TDDB

While Time-Dependent Dielectric Breakdown (TDDB) is a critical reliability topic for front-end devices, TDDB should not be considered strictly a gate oxide issue. An illustration of this point is shown in Figure 5.8-1, where the TDDB lifetime trends versus electric field for different dielectrics of potential use for Back End of Line (BEoL) applications are shown. There are at least a couple of reasons for the emergence of the importance of BEoL TDDB, especially with the recent introduction of so-called low-k dielectrics into the interconnect stack (metallization plus surrounding/supporting dielectrics) **[5.8.1 to 5.8.4.]**. First, while low-k materials enable significant RC performance improvements (i.e., reduced circuit delay) over conventional silica-based BEoL dielectrics, they also possess substantially inferior electrical properties - relative to gate oxide - in terms of leakage and breakdown strength. As seen in Figure 5.8-1, the lower k dielectrics have generally shown poorer TDDB reliability characteristics. Second, InterMetal Dielectric (IMD) spacing between adjacent interconnect metal is approaching the physical dimensions of gate oxides used just a couple of decades ago. Hence, a discussion of what type of physical model for dielectric degradation under electrical stress is important, especially its functional dependence on applied electric field. Earlier work on gate oxides has indicated that TDDB lifetime models are exponentially dependent on field (E or 1/E, see previous discussion on gate oxide TDDB to compare the models). The so-called E model describes TDDB as a bond breaking mechanism, where the applied field can stretch silicon-oxygen (Si-O) bonds thereby weakening them and making them susceptible to thermal breakage. In the case of the 1/E model, the fluence of electrons (that follow a Fowler-Nordheim (F-N) conduction mechanism) is responsible for damage formation within the dielectric. However, F-N conduction is not expected to be significant in the range of electric field strengths typical of at use conditions. Also, since the interconnect electrodes are metals (which have negligible minority carrier contribution), an anode hole injection mechanism may not directly apply. At lower currents, the low-k intrinsic conduction mechanism is expected to be Poole-Frenkel or Schottky so that TDDB lifetime based on a fluence mechanism would need to be based on those conduction mechanisms (and hence is suggested to follow a so-called $\sqrt{(E)}$ type model).

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) ILD/Low-k/Mobile Cu ion (cont'd)

5.8.1 Low-k TDDB (cont'd)

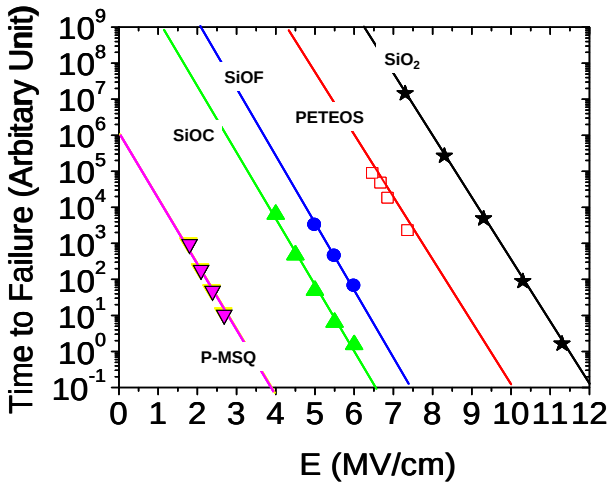


Figure 5.8-1 — Time-Dependent Dielectric Breakdown (TDDB) in various dielectrics [5.8.3].

Plasma-enhanced TEOS (PETEOS) result is taken from **[5.8.2]**. SiO_2 result is for a gate oxide quality dielectric. SiOF, SiOC, and porous-MSQ (P-MSQ) are examples of low-k dielectrics that are used as, or are potential candidates for low-k interconnect dielectrics. The dielectric reliability for BEoL dielectrics shows a decrease in breakdown strength as the value of the low-k dielectric constant decreases.

A field acceleration parameter, γ, can be used to characterize TDDB data over a wide range of electric field strength. γ is empirically determined from the slope of the ln(time-to-failure) versus field plot using the equation listed below for the different models:

E model: $$TTF \propto \exp(-\gamma E) \Rightarrow \gamma = -[\partial \ln(TTF) / \partial E]|_T = \text{Constant} \quad \textbf{(5.8.1)}$$

1/E model: $$TTF \propto \exp(G / E) \Rightarrow \gamma = [\partial \ln(TTF) / \partial E]|_T = G / E^2 \quad \textbf{(5.8.2)}$$

$E^{1/2}$ model: $$TTF \propto \exp(-\alpha\sqrt{E}) \Rightarrow \gamma = -[\partial \ln(TTF) / \partial E]|_T = \alpha / (2\sqrt{E}) \quad \textbf{(5.8.3)}$$

where E is the electric field in the dielectric, T is the fixed temperature at which γ is being determined and TTF is taken to be the characteristic time-to-failure for a TDDB test. G and α are the respective field acceleration parameters in 1/E and $E^{1/2}$ models. The variation of field acceleration parameter with field can be predicted from the above equations. For example, an E model has constant field acceleration parameter with field as described in equation **(5.8.1)**. The other models predict that the observed field acceleration parameter should vary strongly with field, equations **(5.8.2)**, **(5.8.3)**.

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) ILD/Low-k/Mobile Cu ion (cont'd)

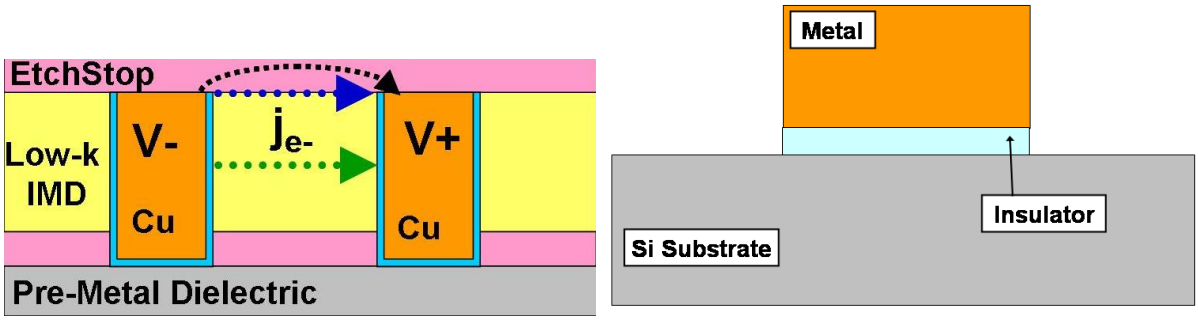
5.8.1 Low-k TDDB (cont'd)

Low-k dielectrics can come in a variety of forms, but the trend in industry has been to adopt materials that are based on a silica (SiO_x) matrix due to process and integration reasons. Silica-based low-k dielectrics have been shown to have inferior breakdown strength and significantly wider failure distributions under constant voltage stress. These trends are attributed to the presence of preexisting defects in the low-k dielectrics that scale roughly with the degree of porosity present within the low-k **[5.8.3]**. Interestingly, low-k TDDB still appears to follow the same degradation physics found in gate oxides; i.e., similar field acceleration parameter γ = ~4 Naperians (natural logarithm) per MV/cm at 105 °C (which yields an effective dipole moment of p_{eff} = ~13 eÅ) **[5.8.3, 5.8.5, 5.8.6, 5.8.8]**, suggesting that the failure of the Si-O bond is a rate-limiting step in the ultimate breakdown of these materials.

Because lower-k valued dielectrics have been obtained by purposely introducing nano-scale voids into the dielectric, the degree of porosity of the material is an important characteristic for assessing dielectric electrical performance. From a reliability perspective, a "pore" in this context is identified as a localized region of low-polarizability with existing weak bonds that may introduce charge traps into the material under electrical stress **[5.8.3]**. Percolation modeling and the assumption of preexisting electrically active defects that scale with the degree of porosity tend to explain both the degraded breakdown strength and wider failure distributions of low-k dielectrics **[5.8.3, 5.8.7]**. Since BEoL processing of the low-k is quite complicated and can necessarily alter the local characteristics of the dielectric, careful assessments of the reliability margins present when using advanced low-k materials are a necessary part of successful process and integration of these new materials. Low-k reliability also should not be considered only an issue in intermetal geometries (as shown in Figure 5.8-2) since interlevel and gate-to-contact geometries may be impacted. Furthermore, extrinsic factors can play a significant role as well. Since a Cu ion is a mobile species under an electric field, any defect that has left or has allowed Cu ions into the dielectric region will enable them to drift between metal electrodes and adversely impact TDDB. The presence of moisture also can have negative impact on interconnect reliability **[5.8.11]**.

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion (cont'd)

5.8.1 Low-k TDDB (cont'd)



(a) IMD configuration for BEoL reliability study (3 paths for electron current flow shown)

(b) MIS structure for Cu ion diffusion study; (for interlevel type configuration)

Figure 5.8-2 — Metal stack cross-section / schematic

5.8.2 TDDB numerical example using E model

Objective: Calculate the acceleration factor (AF) for a low-k dielectric failure by TDDB under use conditions using an E model. The basis for this extrapolation is from test structure lifetime data obtained under stress conditions that accelerate failure.

Assumptions:
Use conditions (temperature & electric field) are: 50 °C & 0.3 MV/cm
Accelerated stress conditions (temperature & electric field) are: 125 °C & 4.0 MV/cm
Field acceleration parameter, γ : 4.0 Naperians (natural logarithm) per MV/cm
Apparent activation energy (nominal value), E_{aa}: 0.75 eV

The ratio of the time-to-failure (TTF) values will be given by the following:

$$AF \text{ (ratio of } TTF_{use} \text{ to } TTF_{accel} \text{ values)} = \exp[-\gamma (E_{use} - E_{accel})] * \exp[(E_{aa} / k)(1 / T_{use} - 1 / T_{accel})]$$

$$AF = \exp[-4.0/(MV/cm)(0.3\ MV/cm - 4\ MV/cm)] *$$

$$\exp[(0.75\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K - 1 / (273 + 125)K)]$$

$$AF = 2.7 \times 10^{6} * 1.6 \times 10^{2} = 4.3 \times 10^{8}$$

Conclusion: Hence, the use lifetime will be ~4×10^8 times longer than observed accelerated stress lifetime. Note that the factor 2,700,000 X is due to the electric field and only a factor 160 X is due to temperature difference.

This example demonstrates the strength of the electric field component of the acceleration in comparison to the temperature component. Thus, if the lifetimes at slightly elevated temperature conditions are experimentally accessible, lifetime projections based on electric field impact can be done near use conditions, if not at the actual use temperature. Certain caveats to accelerated testing are necessary. First, one must be aware that testing under accelerated conditions (higher applied electric field and/or higher temperature) may allow new failure mechanisms to occur that are not intrinsic to the failure channels pertinent near use conditions (e.g., Cu ions in low-k dielectrics become recognizably mobile above 200 °C). Second, the presence of defects (e.g., free Cu) that become highly activated under accelerated conditions can greatly distort lifetime projections, although their detection under such conditions can be viewed as an indicator for further process improvement. Finally, test structure area is generally much smaller than the area of interconnect in real devices.

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion (cont'd)

5.8.2 TDDB numerical example using E model (cont'd)

Thus, knowledge of device area-scaling is usually important and requires detailed understanding of the shape factor associated with the TDDB failure distribution.

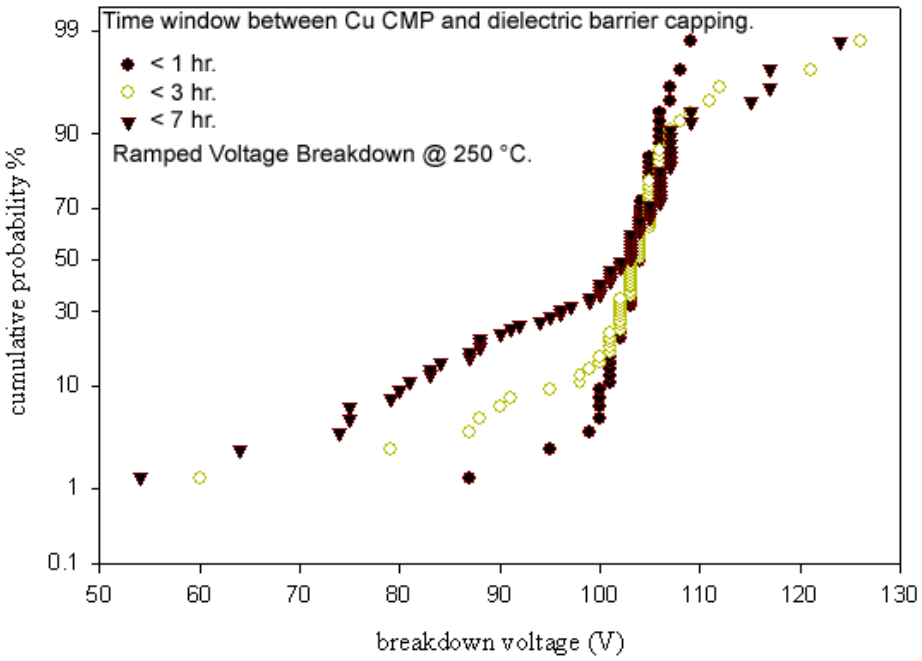


Figure 5.8-3 — Normal Distribution of Breakdown Voltage

Time window between Cu trench CMP and dielectric capping shows significant differences in ramped voltage breakdown, highlighting the importance of ambient exposure in controlling the generation of Cu-induced defects that are made worse by corrosion. Corrosion of exposed Cu leads during processing creates regions of Cu oxide that can extend beyond the confinement of the trenches that normally contain the Cu metallization. After cleaning of the Cu surface to remove any surface oxidation prior to trench encapsulation by a barrier dielectric, the remaining and freshly reduced Cu that has protruded beyond trench confinement can act as a source of mobile Cu ions under electrical stress. Such defects are best detected electrically rather than visually. The data here are derived from a 130 nm Cu/SiOC BEoL technology.

NOTE Many papers in the literature may use and plot base 10 (rather than base e) when expressing the field acceleration factor. One should be careful to note whether base 10 or natural base e is being used. Some authors, for clarity reasons, will write the field acceleration as decades per MV/cm to emphasize that the base 10 is being used or Naperians per MV/cm to emphasize that the natural base e is being used. Many authors, however, may not emphasize this distinction to the reader, so the reader must be cautious. The conversion factor between base 10 and base e is 2.3:1, i.e., $\gamma_{base\ e} = 2.3 * \gamma_{base\ 10}$. In this document, the natural base e is assumed.

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion (cont'd)

5.8.3 Mobile Cu ion in Low-k materials

As previously noted in the section on mobile ions that impact device function, alkaline-metal elements such as Li, Na, and K are especially mobile within dielectrics such as SiO_2 under the presence of modest electric fields (≤1.0 MV/cm) and temperatures (~100 °C). With the successful integration of Cu metallization into the BEoL, mobile Cu ions under electrical bias are a more direct concern - where, for example, loss of trench/via metal barrier or trench dielectric barrier integrity to Cu ion diffusion or the presence of Cu related corrosion defects can lead to substantially degraded backend dielectric reliability performance **[5.8.1, 5.8.9 to 5.8.14]**. Since interfaces are prevalent within Cu interconnect geometries, fast diffusion pathways are potentially available for relatively rapid ion drift. Usually, Cu ion drift under electric field is an issue more for interconnect TDDB than for surface inversion in semiconductor devices. Since such defects are difficult to observe under use conditions, their statistical presence is determined more accurately using accelerated test conditions and relatively rapid tests such as ramped breakdown **[5.8.4, 5.8.11]**. For Cu-based interconnects, the failure mechanism for this rather gross type of failure is viewed essentially as a metal shorting bridge that develops through the local low-k dielectric between two metal electrodes (see Figure 5.8-4).

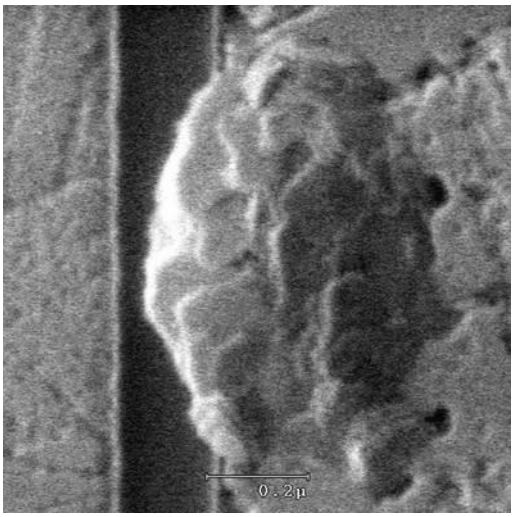


Figure 5.8-4 — Copper short / extrusion

Gross defects can have negative impact on observed TDDB reliability. In the case shown, Cu corrosion has occurred. Post-CMP cleaning of the Cu metallization to remove surface oxide prior to capping dielectric deposition can leave Cu defects that are not completely sealed off from the low-k dielectric by barrier material. Cu ions can then drift across the dielectric region under applied electrical stress and cause premature intermetal dielectric (IMD) failure.

Further comment on the impact of Cu ion defects in a low-k dielectric is warranted here. While the damage described above is similar to the type of discourse generally found in the literature on Cu drift in BEoL dielectrics, the impact of Cu ions on low-k dielectric reliability is best described by distinguishing the relative amounts of Cu ions present within the dielectric matrix itself during electrical stress. At relatively low concentrations, say ~10^{14} to ≤10^{17} ions per cm^3, that are likely typical in low-k dielectrics **[5.8.15]** that have been exposed to Cu CMP but have not been significantly compromised by metal or dielectric barrier failure to contain the Cu metallization, the Cu^+ ion can serve to catalyze the normal Si-O bond breakage process by adding to the local electric field of a Si-O bond.

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion (cont'd)

5.8.3 Mobile Cu ion in Low-k materials (cont'd)

Thus, the Cu^+ ions will have adverse impact on TDDB through the generation of localized point defects that will through the percolation process yield dielectric failure. The generation of this point defect is conceptually similar to how "hole capture" in gate oxide enhances the local field around a Si-O bond **[5.8.8]**.

At this point, there is no consensus about the exact role of Cu in intrinsic dielectric failure and at what concentration the presence of Cu drift overwhelms whatever intrinsic mechanism is driving dielectric breakdown in low-k materials. It is clear, however, that sufficient containment of Cu is essential to ensure interconnect reliability against premature dielectric breakdown and proper dielectric reliability assessment. If barrier containment has failed, then larger scale defects associated with substantial amounts of Cu ionic drift will impact dielectric reliability in two ways: (1) the effective dielectric spacing can be progressively reduced as a local front of Cu ions moves into the dielectric and increases the local electric field; (2) the Cu ion drift leads to a metal bridging defect that shorts the two electrodes. The type of damage depicted in this larger scale damage is typically what is often described in the literature and will be described below. "Large" is defined loosely here as a local Cu contaminated region whose dimension is comparable to and maybe somewhat smaller than the dielectric distance (but not atomic in scale).

The basic physics associated with the drift of mobile Cu ions in low-k dielectrics (at least in the linear approximation $\lambda F / kT << 1$ **[5.8.16]**, where λ is the hopping distance, F is the driving force for the net diffusional flux, k is Boltzman's constant, and T is the temperature) that eventually bridges the dielectric should be essentially the same as that for mobile species that affect device-level function (see 5.4 on surface inversion). This analysis is based on a particular form of Fick's First Law that includes contributions from stress-assisted diffusion **[5.8.17]**. The mobile ion flux is controlled by the electric field strength and temperature. Thus, the time-to-failure (TTF) can be written to have a form as:

$$TTF = A * (< J_{ion} >)^{-1} * \exp(E_{aa} / kT) \qquad \textbf{(5.8.4)}$$

where

A	=	material dependent constant
$< J_{ion} >$	=	is the time-averaged mobile ion flux
E_{aa}	=	apparent activation energy for mobile ion diffusion (0.75 to 1.8 eV)
k	=	Boltzmann's constant
T	=	temperature in kelvins

and

$$< J_{ion} > = < (e E) * \rho(x,t) * (D_o / kT) - (D_o \, \partial\rho(x,t) / \partial x) > \qquad \textbf{(5.7.5)}$$

where the time-averaged mobile ion flux $< J_{ion} >$ has two components:

1. $(e E \rho D_o / kT)$ is the drift component which cause surface inversion during device operation, where:
   - e is the electronic charge on the mobile ion
   - E is the externally applied electric field across dielectric
   - ρ is the mobile ion density
   - D_o is the diffusion coefficient
2. $(D_o \, \partial\rho(x,t) / \partial x)$ is the back diffusion component (or recovery component).

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion (cont'd)

5.8.3 Mobile Cu ion in Low-k materials (cont'd)

If the electric field is turned off and the device is baked (i.e., an unbiased bake), it is possible that J_{ion} can change direction (i.e., will now be dominated by back diffusion) and the device may exhibit some degree of recovery, known as "bake-recovery fails"; however, it is also likely that in the BEoL, the migrating ions can recombine with electrons from the cathode and subsequently "plate-out" (see Figures in **[5.8.12, 5.8.18]**) and block out the possibility of such bake-recovery.

A net velocity of ionic drift $V_{ion}(x,t)$ is found by dividing $J_{ion}(x,t)$ by the ionic concentration $\rho(x,t)$. Thus, a more explicit representation of a time-to-failure is roughly given by the (dielectric thickness) / $V_{ion}(x,t)$.

Again, there are strong caveats here. First, this expression is an approximation. For example, if sufficient plating-out of metal occurs, then the actual dielectric spacing before failure is likely smaller than the nominal dielectric thickness, and the actual nominal electric field during stress can increase with time. Second, the assumption that equation **(5.8.5)** is valid for all temperatures and fields (i.e., λ F / kT << 1) is not correct. For example, if the hopping distance is about 7 Å, and an electric field of 0.2 MV/cm is applied across a dielectric, equation **(5.8.5)** will not be valid at 50 °C but will be closer to valid at 250 °C. Generally, a more sophisticated expression for drift diffusion will be necessary for accurate acceleration factor determination and lifetime prediction; however, no clear consensus on the most relevant model is yet to be established **[5.8.9, 5.8.13 to 5.8.16]**.

The activation energy, E_{aa}, depends upon the ULSI medium through which the ion must diffuse and for Na^+ ions it ranges from 0.75 to 1.8 eV, with 1.0 eV being typical.

NOTE In surface inversion, it is noted that Stuart finds 0.75 eV for Na (theory and experiment) and ~1.1 eV or more for everything else. For Cu diffusion into dielectrics, different authors estimate different values ranging from about 0.8 eV to as high as 1.8 eV, depending on the test structure, test methodology, and types of dielectrics used **[5.8.19 to 5.8.22]**. Hence, a nominal value of about 1.0 eV for Cu ionic drift diffusion does not seem out of bounds for this discussion.

5.8.4 Mobile Cu ion numerical example

Objective: Calculate a simple (but not necessarily accurate) estimate of the acceleration factor (AF) for Cu ion drift under use environment conditions compared to an accelerated stress environment.

Assumptions:
The use temperature and electric field conditions are: 50 °C chip temperature & E = 1.0 MV/cm
The accelerated stress temperature and electric field conditions are: 250 °C & E = 4.0 MV/cm
$[Cu^{+n}]$ at failure = 10^{18} ions per cm^3 (use & accelerated stress conditions)
Apparent activation energy, E_{aa} = 1.0 eV

NOTE The metal spacing is the same in both cases and its value is not necessary for the calculation below. The ionic concentration at failure is expected to be similar at both conditions by assuming that the low-k dielectric is relatively clean before stress and then is contaminated by a large concentration of Cu ions during electrical and temperature stress through some type of defect.

It is demonstrated in the literature that Cu drift diffusion into dielectric dominates simple diffusion **[5.8.19 to 5.8.22]**, and calculations here also agree with this observation.

5.8 BEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – ILD/Low-k/Mobile Cu ion (cont'd)

5.8.4 Mobile Cu ion numerical example (cont'd)

For a fixed test condition (temperature and electric field), the ratio of the drift flux to the back diffusion flux is roughly given by: (e E / kT) / (1 / dielectric spacing), at least initially. If the electric field is 4.0 MV/cm at 250 °C for an interconnect spacing of 90 nm, then the ratio is about:
$\{(4.0 \times 10^{6}$ eV/cm) / $[(8.62 \times 10^{-5}$ eV/K)((273 + 250)K)]$\}$ * $(90 \times 10^{-7}$ cm) = ~800, indicating that the drift term is nearly 1000 X stronger than the diffusion term initially. Of course, as the effective spacing decreases during stress due to Cu diffusion, the back diffusion term may become more important, but its role is generally ignored because the detrimental effects of ionic drift to circuit function are a more important consideration. The small spacing needed to enhance the concentration gradient for back diffusion will likely be in the regime where the device malfunctions, although this might be a source of future debate. As the temperature decreases, this ratio will increase so that drift will continue to dominate under use conditions.

Ignoring the back diffusion component, the ratio of the TTF values can be estimated. Note that the diffusion pre-exponent factor D_o will cancel out, but contributions in the form of electric field and temperature ratios will remain along with the necessary Arsenics term:

Ignoring back diffusion, $J_{ion} = \sim(e\,E) * (\rho\, D_o / kT)$

$$AF \text{ (ratio of } TTF_{use} \text{ to } TTF_{accel} \text{ values)} = (J_{ion,\,use} / J_{ion,\,accel})^{-1} \exp[(E_{aa} / k)(1 / T_{use} - 1 / T_{accel})]$$

$$AF = (E_{accel} / E_{use})(T_{use} / T_{accel}) * \exp[(E_{aa} / k)(1 / T_{use} - 1 / T_{accel})]$$

$$AF = (4.0 \text{ MV/cm} / 1.0 \text{ MV/cm})((273 + 50)K / (273 + 250)K) *$$

$$\exp[(1.0 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 50)K - 1 / (273 + 250)K)]$$

$$AF = 4.0 * 0.6176 * 9.223 \times 10^{5} = \sim 2.3 \times 10^{6}$$

Conclusion: The estimated impact of the accelerated stress environment to use conditions in a defect dominated sample will only increase the TTF value by $\sim 2.3 \times 10^{6}$ times the accelerated stress value. The difference here is that the drift factor has only linear dependence on the electric field and hence minimal impact on the overall acceleration factor while the contributing Arrhenius factor is nearly 1,000,000 X. While this example is best considered as illustrative rather than quantitative, this low acceleration factor value would be of concern if the intrinsic BEoL TDDB reliability is masked by substantial amounts of Cu contamination.

5.9 BEoL Failure Mechanisms – Aluminum Electromigration (Al EM)

5.9.1 Electromigration in long metal lines

Due to momentum exchange between the current-carrying electrons and the host metal lattice, aluminum ions can drift in the direction of the electron current **[5.9.1]**. In the presence of flux divergent sites, this drift induces a stress gradient that at steady state is proportional to the current density. Citation **[5.9.2]** notes that in sufficiently long conductors and at high current densities, the stress will increase to the point where voids will form in regions of tensile stress that subsequently grow to the point of failure. It is also possible that at locations of high compressive stress extrusions and hillocks can form that can cause failure of the protective passivation or induce short circuits.

5.9.1.1 Constraints and limitations for EM in long metal lines [5.9.5 to 5.9.22]

For Al-alloy stripes having no barrier metallization, the total time-to-failure for 50% cumulative (t_{50}) is dominated by nucleation which produces current density exponent, n, in Black's Equation, $t_{50} = A * j^{-n} * \exp(E_{aa} / kT)$, which is observed to be equal to 2 **[5.9.3]**. E_{aa} is the apparent activation energy, T is absolute temperature in kelvins and k is Boltzmann's constant.

For Al-alloy stripes on barrier metal and terminated by tungsten plugs, one may see both an incubation (nucleation) period, dominated by n = 2, and a resistance rise (drift period) dominated by n = 1 or a blend of both current exponents to produce an intermediate value. Larger n values can be observed if Joule heating and/or geometry are not properly considered **[5.9.4]**.

Under high current density test conditions, unaccounted for self-heating can produce temperature gradients that induce **apparent** current density exponents **much** greater than 2. Thus, extreme care must be taken when extrapolating time-to-failure data from high to low current densities. The amount of Joule heating should be limited to less than 5 °C at stress conditions to obviate temperature gradient induced failure.

The industry standard NIST bow-tie type EM test structure with simple bonding pad connections is grossly inadequate for present multilevel metal systems and generally gives overly optimistic EM results relative to via-fed test structures.

EM kinetics for both lines and vias may be different according to linewidth. This is due to the presence or absence of a continuous grain-boundary network that would provide a continuous pathway for diffusion.

Via-fed test structures must be carefully designed to avoid resistance saturation and reservoir effects, which can produce misleading t_{50} and σ values.

The test temperature must be limited to a regime where the transport mechanism is the same at test conditions as is at use conditions (grain-boundary vs lattice diffusion). In addition, the equilibrium microstructure must also be nearly the same (phase diagram). Thus to maintain relevance, the test temperatures should not exceed ~250 °C including Joule heating.

If the preceding are not considered, it will be impossible to extrapolate test conditions to use conditions and in most cases the erroneous predictions will be optimistic.

5.9.1 Electromigration in long metal lines (cont'd)

5.9.1.2 Constraints and limitations for EM in vias and contacts

Electromigration associated with vias and contacts must be investigated separately because they show characteristics unlike single leads fed by bond pads **[5.9.5 to 5.9.7]**. Vias can show different degradation rates depending on electron current flow direction (M2-to-M1 versus M1-to-M2) and the degradation rate is strongly dependent on via structure, via number, and layout. Via degradation may also have a reservoir effect.

Silicide formation and barrier type are extremely important for contact electromigration. Silicon (not aluminum) may be the dominant diffusing species for contact failure if there is no diffusion barrier between the conductor and the silicon.

5.9.2 Models

The model generally accepted to describe median time-to-failure (TTF) takes the form **[5.9.5]**:

$$TTF = A_o * (J - J_{crit})^{-n} * \exp(E_{aa} / kT) \qquad \textbf{(5.9.1)}$$

where

- A_o = arbitrary scale factor
- J = applied current density
- J_{crit} = the current density below which no electromigration takes place in the specific structure being tested
- n = current density exponent
- E_{aa} = apparent activation energy in electronvolts (eV)
- k = Boltzmann's constant
- T = temperature in kelvins

In this model, J must be much greater than J_{crit} to produce failure that can be meaningfully extrapolated to a use condition. J is the average current density $< J >$ **[5.9.13, 5.9.14]**. The current density should be averaged over a period of the order of the jump frequency of a diffusing atom, at test conditions on the order of a millisecond.

It must be stressed that the definition of a long line must be that the line is substantially longer than the Blech length for the current density applied. If line length is not more than several times the Blech length, then large apparent n values can be obtained from tests.

The Blech length and the critical current density are related according to the Blech relationship $L_b \times J_{crit}$ = constant, which for Al alloys is on the order of 3,000 to 7,000 A/cm depending upon the materials chosen for the interlevel dielectric. Stronger dielectrics with good adhesion exhibit higher values then weaker dielectrics with poor adhesion. From these considerations, for test current densities on the order of 10 mA/μm^2 (1×10^6 A/cm^2), the conductor should be at least 500 μm in length and preferably 1 mm long.

Failure criteria should be the smallest resistance increase that can be reliably measured. Failure criteria that depend on product requirements are problematic since the resistance increase that can be expected from a void will be a sensitive function of geometry and therefore serendipitous. Layered metal systems will exhibit n = 2 for the incubation period followed by n = 1 for resistance growth.

Commonly accepted activation energies are:

E_{aa} = 0.5 to 0.6 eV for Al and Al + small %Si.

E_{aa} = 0.7 to 0.8 eV for Al + Al alloys doped with a small %Cu.

E_{aa} = 0.9 eV for fine line (bamboo structure) Al alloys deposited onto redundant barrier metals.

5.9 BEoL Failure Mechanisms – Aluminum Electromigration (Al EM) (cont'd)

5.9.3 Electromigration numerical example

Objective: Calculate the acceleration factor (AF) in a Mobile environment vs. an Office environment.

Assumptions:
Very long Al-Cu metalization stripes with large grain size vs. line width (bamboo)
Mobile conditions are: 80 °C chip temperature (inside the laptop PC) & 2.5 x 10^5 A/cm^2 current density
Office conditions are: 50 °C chip temperature (inside the desktop PC) & 2.0 x 10^5 A/cm^2 current density
Apparent activation energy, E_{aa}: 0.8 eV
$J >> J_{crit}$ and n = 2

AF, the ratio of the time-to-failure (TTF) values will be:

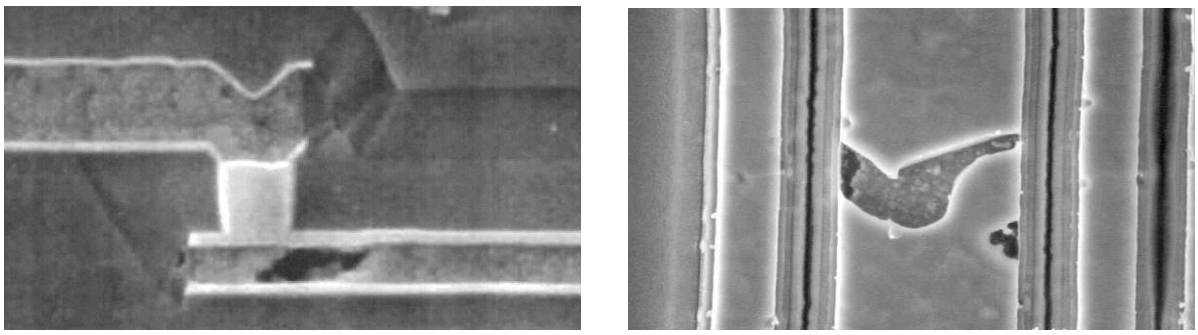
$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{mobile} \text{ values)} = (J_{office} / J_{mobile})^{-n} * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{mobile})]$$

$$AF = (2.0 / 2.5)^{-2} * \exp[(0.8 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 50)\text{K} - 1 / (273 + 80)\text{K})]$$

$$AF = 1.56 * 11.5 = 18$$

Conclusion: Moving from the hot, high current density Mobile environment to the cool, low current density Office environment will increase the TTF value to about 18 X that of the previous value. Current density accounts for ~1.6-fold, while temperature accounts for a factor of ~12; therefore, the overall increase in lifetime at Office (lower) conditions is close to 20 times.

5.9.4 Examples of aluminum electromigration



(a) cross-section of via interconnect with extensive electromigration

(b) aluminum line electromigration

Figure 5.9-1 — Examples of aluminum electromigration

5.10 BEoL Failure Mechanisms – Copper Electromigration (Cu EM)

As in the case of aluminum (Al), momentum exchange between current-carrying electrons and copper (Cu) ions in a Cu line cause Cu ions to drift in the direction of the electron current. In the presence of flux divergence sites where the flux of Cu atoms into the site is unequal to the flux leaving the site, a stress gradient is induced that is proportional to the current density, and can be tensile or compressive, depending on the sign of the divergence. In sufficiently long conductors with sufficiently high current densities, the tensile stress at a negative divergence site will increase to the point where voids will form due to vacancy coalescence, and will grow until they are large enough to cause failure. Compressive stress at sites of positive divergence will cause the formation of extrusions and hillocks that can cause cracking in the protective passivation, and short circuiting of neighboring conductors due to extruded Cu **[5.10.1 to 5.10.8]**.

5.10.1 Constraints and limitations

In contrast to Al, Cu lines with a refractory liner and terminated by dual-damascene Cu vias, little or insignificant incubation time (time required before a void nucleates) is observed. Therefore, for Cu technologies, the current density exponent, n, is ~1.1, very close to 1. Why the exponent is not exactly equal to 1 is presently unknown, but may be an effect of non-metallic impurities present in the Cu. In some structures, the value of n may be greater than 1.1 but less than 2. The reason for the higher value is also not understood, but appears not to be a consequence of Joule heating **[5.10.4]**.

Under high current density test conditions, unaccounted for self-heating can produce apparent current density exponents greater than 2, and extrapolation of time-to-failure data from high to low current densities must take this into account.

EM kinetics for lines and vias may be different due to differences in the density and location of Cu grain boundaries or other mass transport paths in the lines as compared with the vias, and should be checked separately **[5.10.4]**.

As with Al, single level EM lines with simple bonding pad connections produce much longer lifetimes than via-fed test structures, and can therefore produce overly optimistic lifetime projections compared to results from via-fed test structures. In addition, such structures rarely exist in practice, and via-terminated test structures are more representative of product designs.

Via-terminated test structure lifetime distributions are influenced by electron flow direction due to asymmetric processing (M2-to-M1 versus M1-to-M2, and should be tested both ways. Via-terminated test structures must be carefully designed to avoid resistance saturation and reservoir effects, which can produce misleading t_{50} and σ values **[5.10.5]**. Via-terminated test structure lifetime distributions are also influenced by the number and arrangement (layout) of vias; the designer needs to account for resistance and saturation effects **[5.10.6]**.

5.10 BEoL Failure Mechanisms – Copper Electromigration (Cu EM) (cont'd)

5.10.2 Models

The model generally accepted to describe median time-to-failure (TTF) follows Black's Law **[5.10.7]**, same as aluminum **[5.9.3 to 5.9.9, 5.10.8]**:

$$TTF = A_o * (J - J_{crit})^{-n} * \exp(E_{aa} / kT) \quad \textbf{(5.10.1)}$$

where

- A_o = arbitrary scale factor
- J = applied current density
- J_{crit} = the current density below which no electromigration takes place in the specific structure being tested
- n = current density exponent
- E_{aa} = apparent activation energy in electronvolts (eV)
- k = Boltzmann's constant
- T = temperature in kelvins

J_{crit} is obtained from the Blech relationship L_b x J_{crit} = constant, where L_b is the Blech length; for Cu, the resulting product is ~3000 A/cm. J must be much greater than J_{crit} to produce failure in a reasonably short (days) time, and that can be extrapolated to use conditions.

Structures being stressed to determine the minimum lifetime must be substantially longer than the Blech length for the current density applied during stress. If line length is not more than several times the Blech length, then large apparent n values can be obtained from tests. Test structure lengths are commonly between 200 and 400 μm for stress current densities on the order of 20 mA/μm^2.

The failure criterion is a fractional or percentage resistance increase (e.g., $\Delta R / R$ x 100 = 20% is commonly used). Cu resistance vs. time R(t) curves behave differently than those for Al. Whereas Al structures show a short inactive period (no resistance shift) due mostly to incubation time, followed by a linear resistance increase with time, Cu curves show a longer initial inactive period followed by a rapid jump in resistance, and then by a linear increase in resistance with time. The choice of failue criterion should be made such that it samples one or the other (but not both) of these behavioral regions in order to avoid producing a bimodal failure distribution.

Cu via / line test structures will exhibit $1.1 < n < 2$ with E_{aa} = 0.85 to 0.95 eV for Cu EM **[5.10.3]**.

5.10.3 Electromigration numerical example

Objective: Calculate the acceleration factor (AF) in a Mobile environment vs. an Office environment.

Assumptions:
Very long Cu metalization stripes with large grain size vs. line width (bamboo)
Mobile conditions are: 80 °C chip temperature (inside the laptop PC) & 2.5 x 10^5 A/cm^2 current density
Office conditions are: 50 °C chip temperature (inside the desktop PC) & 2.0 x 10^5 A/cm^2 current density
Apparent activation energy, E_{aa}: 0.9 eV
$J >> J_{crit}$ and n = 1.1

AF, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{mobile} \text{ values)} = (J_{office} / J_{mobile})^{-n} * \exp[(E_{aa} / k)(1/ T_{office} - 1/ T_{mobile})]$$

$$AF = (2.0 / 2.5)^{-1.1} * \exp[(0.9 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 50)K - 1 / (273 + 80)K)]$$

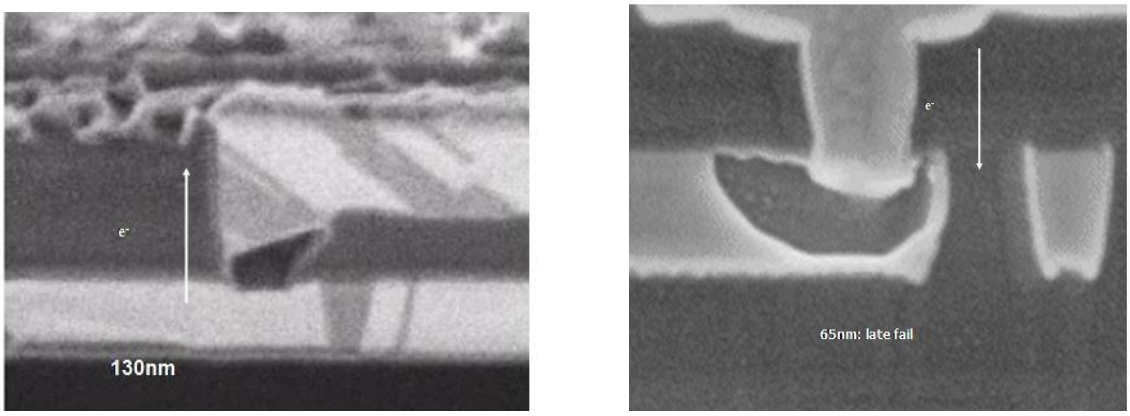
$$AF = 1.28 * 15.6 = 20$$

5.10 Copper Electromigration (Cu EM) (cont'd)

5.10.3 Electromigration numerical example (cont'd)

Conclusion: Moving from the hot, high current density Mobile environment to the cool, low current density Office environment will increase the TTF value to about 20 X that of the previous value. Current density accelerates failure by ~1.3 times, while temperature accelerates failure by ~16 times; therefore, the overall increase in lifetime at Office (lower) conditions is about 20 times.

5.10.4 Examples of Copper Electromigration



(a) EM void in a Cu via over the line (electrons flowing up)

(b) EM void in a Cu line under a via (electrons flowing down)

Figure 5.10-1 — Examples of Copper Electromigration

5.11 BEoL Failure Mechanisms – Aluminum and Copper Corrosion

Corrosion failures can occur when ULSI devices are exposed to moisture and contaminants **[5.11.1 to 5.11.11]**. Corrosion failures are usually classified as one of two broad groups: bonding pad corrosion or internal chip corrosion. Bonding pad corrosion (see Figure 5.11-1) is usually more common simply because the die passivation does not cover the metallization in the bonding pad locations. Internal chip corrosion (internal to the chip, away from the bonding pads) can also occur if some weakness or damage exists in the die passivation which would permit the moisture and contaminants (e.g., chlorine ions) to reach the metallization.

Corrosion can generally be described in terms of a "corrosion cell" where there must be four key components in order for corrosion to occur: an anode, a cathode, an electrolyte, and a conductor to provide a path for the electron flow needed for the oxidation/reduction processes. An example of "wet" corrosion is shown in Figure 5.11-2. Metal corrosion (oxidation) can occur if there is an imperfection in the native oxide covering the metallization. Generally, Al forms a good self-passivating oxide and is much less corrosive than Cu, even though the Galvanic series would suggest just the opposite. However, if chlorine ions are added to water, then the Al_2O_3 native oxide protecting the Al will be quickly reduced, thus exposing a highly reactive virgin Al surface which will then rapidly corrode **[5.11.6]**.

In order for the corrosion to continue at a rapid rate, the contaminants and metal ions must be able to diffuse rapidly to and from the corroded region, respectively. This can occur easily in liquids and the activation energy for liquid/wet corrosion is generally very low (~0.3 eV). However, for "dry" or "ambient" corrosion (see Figure 5.11-3), the activation energy for diffusion is generally higher and the corrosion rate is very dependent on the percent relative humidity (%RH). In fact, the surface mobility has been shown to be exponentially dependent on %RH over a rather wide range of humidity conditions **[5.11.3]**.

5.11 BEoL Failure Mechanisms – Aluminum and Copper Corrosion (cont'd)

Industry standard tests have been developed and are used to accelerate potential ULSI corrosion failure mechanisms: 85/85 (biased, 85 °C and 85%RH), autoclave (unbiased, 121 °C and 100%RH), and highly accelerated stress test (HAST) (biased, 121 °C and 85%RH), and Unbiased Highly Accelerated Stress Test (UHAST) (Unbiased, 121 °C and 85%RH). . To extrapolate accelerated corrosion results to field use conditions, at least three models have been reported and used. The time-to-failure (TTF) and the acceleration factor (AF) are given below for each of the three corrosion models. Historical citations still of value are **[5.11.12 to 5.11.22]**.

5.11.1 Constraints and limitations

Industry consensus is that the proper activation energy for aluminum corrosion is in the 0.7 to 0.8 eV range if chloride is the agent.

There is not a consensus for the humidity dependence due to lack of data below 85%RH. The relevant relative humidity (RH) is a local RH, the RH found at the interface between the Si chip and the package, which is not necessarily the ambient RH. If power dissipation is small, then ambient RH is approximately the same as local RH. If the power dissipation is large, stress tests may need to employ a duty cycle <100% **[5.11.17, 5.11.18]** to align local and ambient RH values well enough to get meaningful data.

5.11.2 Models

5.11.2.1 Reciprocal exponential humidity model [5.11.7, 5.11.15]

The time-to-failure (TTF) is expressed as:

$$TTF = A_o * \exp(b / RH) * \exp(E_{aa} / kT) \quad \textbf{(5.11.1)}$$

where

- A_o = arbitrary scale factor, dependent upon materials & process details
- b = reciprocal humidity dependence parameter; ~300% if phosphoric acid present **[5.11.7]**, but ~529% for modern processes w/ chloride as the agent **[5.11.15]**
- RH = relative humidity expressed as a percentage, % (Note: 100% = saturated)
- E_{aa} = apparent activation energy, 0.3 eV if phosphoric acid present **[5.11.7]**, but ~0.75 eV for modern processes w/ chloride as the agent **[5.11.15]**
- k = Boltzmann's constant
- T = temperature in kelvins

When extrapolating accelerated failure data from higher humidity $(RH)_{high}$ and higher temperature T_{high} stress conditions to some lower relative humidity $(RH)_{low}$ and lower temperature T_{low} use conditions, the acceleration factor (AF) associated with this model becomes:

$$AF = \exp[b * (1 / (RH)_{low} - 1 / (RH)_{high})] * \exp[(E_{aa} / k)(1 / T_{low} - 1 / T_{high})] \quad \textbf{(5.11.2)}$$

5.11.2 Models (cont'd)

5.11.2.2 Power-law humidity model [5.11.8]:

The time-to-failure (TTF) is expressed as:

$$TTF = A_o * (RH)^{-n} * \exp(E_{aa} / kT) \quad \textbf{(5.11.3)}$$

where

- A_o = arbitrary scale factor, dependent upon materials & process details
- RH = relative humidity expressed as a percentage, % (Note: 100% = saturated)
- n = Peck RH exponent, 2.7 (experimentally determined for Al corrosion)
- E_{aa} = apparent activation energy, 0.7 to 0.8 eV (typical for aluminum corrosion when chlorides are present)
- k = Boltzmann's constant
- T = temperature in kelvins

When extrapolating accelerated failure data from higher humidity $(RH)_{high}$ and higher temperature T_{high} stress conditions to some lower relative humidity $(RH)_{low}$ and lower temperature T_{low} use conditions, the acceleration factor (AF) associated with this model becomes:

$$AF = [(RH)_{high} / (RH)_{low}]^n * \exp[(E_{aa} / k)*(1 / T_{low} - 1 / T_{high})] \quad \textbf{(5.11.4)}$$

5.11.2.3 Exponential humidity model [5.11.3, 5.11.9, 5.11.10]:

The time-to-failure (TTF) is expressed as:

$$TTF = A_o * \exp(-a * RH) * \exp(E_{aa} / kT) \quad \textbf{(5.11.5)}$$

where

- A_o = arbitrary scale factor, dependent upon materials & process details
- a = 0.10 to 0.15 $(\%)^{-1}$
- RH = relative humidity expressed as a percentage, % (Note: 100% = saturated)
- E_{aa} = apparent activation energy, 0.7 to 0.8 eV (typical for aluminum corrosion when chlorides are present)
- k = Boltzmann's constant
- T = temperature in kelvins

The acceleration factor (AF) associated with this model becomes:

$$AF = \exp\{a * [(RH)_{high} - (RH)_{low}]\} * \exp[(E_{aa} / k)(1 / T_{low} - 1 / T_{high})] \quad \textbf{(5.11.6)}$$

5.11.2.4 Lawson humidity model [5.11.16]:

The Lawson model integrates a fitted parameter for %RH as a sum with the Arrhenius portion of the acceleration model. It adds in a fit factor , and the acceleration factor becomes:

$$AF = \exp\{[(E_{aa} / k)(1 / T_{low} - 1 / T_{high}) + b * [(RH_{high})^2 - (RH_{low})^2]\} \quad \textbf{(5.11.7)}$$

where

- b = 4.4e-4, dependent on corrosion specifics
- RH = relative humidity expressed as a percentage, % (Note: 100% = saturated)
- E_{aa} = apparent activation energy, 0.64eV, dependent on corrosion specifics
- k = Boltzmann's constant
- T = temperature in kelvins

5.11 BEoL Failure Mechanisms – Aluminum and Copper Corrosion (cont'd)

5.11.3 Corrosion numerical example

Objective: Calculate the acceleration factor (AF) for Al corrosion (bond pads) due to chloride contamination for an office environment vs. a HAST environment.

Assumptions:

The office temperature, RH, and bias conditions are: 50 °C chip temperature, 10%RH at chip surface (this could be consistent with room environment at 20 °C/50%RH), & V_{office} = 5.0 V

The HAST temperature, RH, and bias conditions are: 130 °C, 85%RH inside the stress chamber, & V_{HAST} = 6.0 V

Peck RH exponent: 2.7, which was experimentally determined for Al corrosion

Corrosion rate is linear with applied voltage

Apparent activation energy, E_{aa}: 0.75 eV

Using equation **(5.10.3)**, the acceleration factor (AF) becomes:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{HAST} \text{ values)} = [(RH)_{HAST} / (RH)_{office}]^{n} * (V_{HAST} / V_{office}) * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{HAST})]$$

$$AF = [85\%RH / 10\%RH]^{2.7} * (6.0\ V / 5.0\ V) * \exp[(0.75\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K - 1 / (273 + 130)K)]$$

$$AF = 323 * 1.2 * 210 = \sim 8.15 \times 10^{4}$$

Conclusion: Moving from a HAST environment to the office environment will increase TTF value to 82,000 times the accelerated stress (HAST) value, of which 323 X is due to RH, 1.2 X is due to applied voltage, and 210 X is due to temperature.

Consensus: In conclusion, there seems to be reasonably good consensus in the industry that the proper activation energy, E_{aa} to use for chloride-induced aluminum corrosion is in the range of 0.7 to 0.8 eV. There is not a consensus for the humidity dependence. A comparison of the three models **[5.11.10, 5.11.11]** tended to favor the exponential model with an a value of ~0.12 to 0.15 $(\%)^{-1}$. However, currently, the inherent simplicity of the power-law model makes it the most widely used corrosion model in the industry.

5.11 BEoL Failure Mechanisms – Aluminum and Copper Corrosion (cont'd)

5.11.4 Example of corrosion and reaction processes

Corrosion of aluminum bonding pads can occur if chlorides and moisture are present.

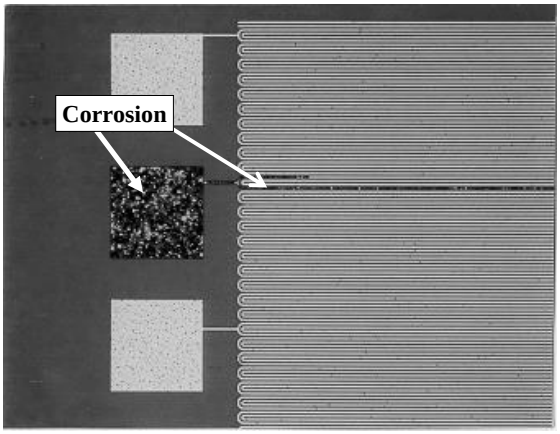


Figure 5.11-1 — Aluminum bond pad corrosion

"Wet" corrosion generally occurs with a low activation energy because of the very high mobility of the diffusing species in water. Note that the four necessary components of the corrosion cell are present: anode, cathode, electrolyte, and a conductor for electron movement.

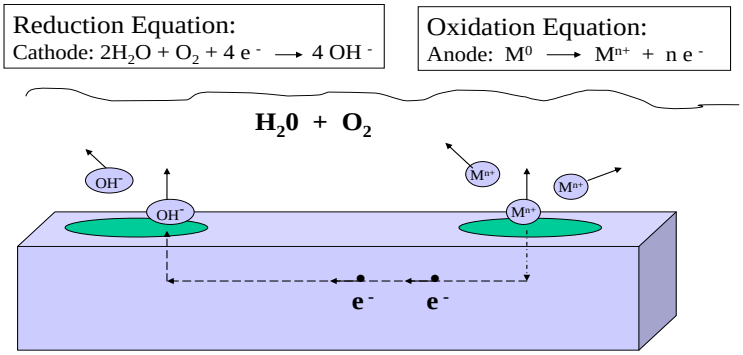


Figure 5.11-2 — Electrochemical reaction

"Dry" or ambient corrosion is strongly humidity dependent because the percent relative humidity (%RH) greatly impacts surface/interface mobility of the diffusing species.

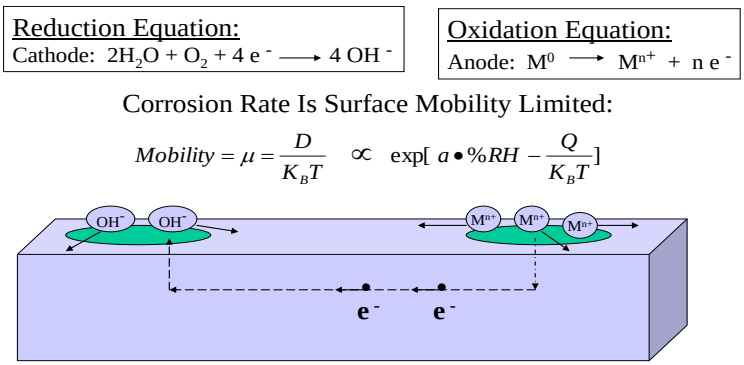


Figure 5.11-3 — Corrosion rate versus surface mobility

5.12 BEoL Failure Mechanisms – Aluminum Stress Migration (Al SM)

The term stress migration describes the movement of metal atoms under the influence of mechanical stress gradients. Generally, stress gradients can be assumed to be proportional to the applied mechanical stress. Vacancies diffuse from sites of small hydrostatic stress to high stress regions to effect metal movement. Flux divergence associated with the metal movement causes voiding in the ULSI metal leads. The resistance rise associated with the void formation may cause electrical failures **[5.12.1 to 5.12.7]**.

The role of stress and stress relaxation is very important in the nucleation and growth of voids in Al-alloy interconnects. Cu doping in the aluminum is somewhat effective in suppressing grain-boundary diffusion, but is much less effective if the grain size is large compared to linewidth, i.e., bamboo leads, as one observes slit-like void formation due to intra-grain diffusion.

5.12.1 Constraints and limitations

This model applies to aluminum alloys (doped with Cu and/or Si) only; Copper SM is discussed in 5.13.

Currently, there is no standard industry test for SM. Typically, long (>1000 μm) and narrow (<2 μm width) stripes are stored (unbiased) at temperatures of 150 to 250 °C for 1000 to 2000 hours and then electrically tested for resistance increases or reduction in breakdown currents. Electromigration stressing is optional after SM baking.

The SM baking temperature should be carefully selected because the maximum creep rate is generally in the range between 150 °C and 250 °C. The maximum in the creep rate occurs due to the high stress but low mobility at low temperatures, and low stress but high mobility at high temperatures.

Because the mechanical stress is temperature dependent, a straightforward determination of the diffusional activation energy is difficult to obtain. Generally, an E_{aa} of ~0.5 to 0.7 eV is used for grain-boundary diffusion and 1.2 to 1.4 eV for single-grain (bamboo-like) diffusion (although intra-grain diffusion can be as low as 1 eV with Cu additions to Al).

The use of refractory metal barriers or layered metallization tends to nullify the severe damage caused by slit-like void formation in bamboo leads. The refractory metal layer acts as a redundant conductor, shunting the current and reducing the electrical resistance rise due to the void formation.

5.12.2 Models

5.12.2.1 Mechanical stress model

The time-to-failure (TTF) can use an Eyring model, for which one computes the product of a power-law on mechanical stress and an Arrhenius factor **[5.12.2, 5.12.3]**.

$$TTF = B_o * (\sigma)^{-N} * \exp(E_{aa} / kT) \qquad \textbf{(5.12.1)}$$

where

- B_o = pre-factor
- σ = constant stress load
- N = 2 to 3 for ductile metals
- E_{aa} = apparent activation energy, 0.5 to 0.6 eV for grain-boundary diffusion; ~1 eV for single-grain (bamboo-like) diffusion
- k = Boltzmann's constant
- T = temperature in kelvins

5.12 BEoL Failure Mechanisms – Aluminum Stress Migration (Al SM) (cont'd)

5.12.2 Models (cont'd)

5.12.2.2 Thermomechanical stress model

If the stress is generated by differing thermal expansion rates, then the stress is called "thermomechanical stress" and is proportional to the change in temperature, i.e., thermal strain, $\varepsilon \propto (\Delta T)$ that then drives σ, stress.

Therefore, the time-to-failure can be written **[5.12.2, 5.12.3]**:

$$TTF = B_o * (T_o - T)^{-N} * \exp(E_{aa} / kT) \qquad \textbf{(5.12.2)}$$

where

B_o	=	pre-factor
T_o	=	stress-free temperature for metal (approximate metal deposition temperature for aluminum)
N	=	2 to 3 for ductile metals
E_{aa}	=	apparent activation energy, 0.5 to 0.7 eV for grain-boundary diffusion; 1.2 to 1.4 eV for intra-grain diffusion
k	=	Boltzmann's constant
T	=	temperature in kelvin

5.12.3 Stress migration numerical example

Objective: Calculate the acceleration factor (AF) for stress migration in an office environment vs. an accelerated stress environment.

Assumptions:
Office conditions are: 50 °C chip temperature inside the enclosure
Accelerated conditions are: 150 °C stress temperature
T_o = 300 °C
N = 2.5
E_{aa} = 0.55 eV

AF, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = [(T_o - T_{office}) / (T_o - T_{accel})]^{-N} * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{accel})]$$

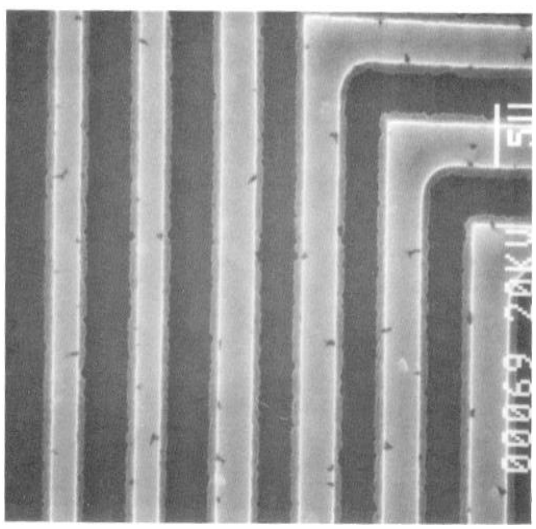
$$AF = [(300 - 50) / (300 - 150)]^{-2.5} * \exp[(0.55 \text{ eV} / 8.62\text{x}10^{-5} \text{ eV/K})(1 / (273 + 50)\text{K} - 1 / (273 + 150)\text{K})]$$

$$AF = 0.28 * 107 = 30$$

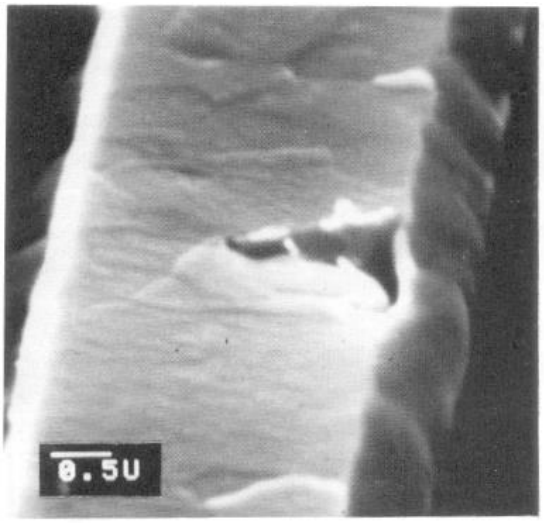
Conclusion: Moving from the accelerated environment to the office environment will increase TTF value to about 30-fold that of the accelerated stress value. Mechanical stress decreases the TTF value by ~0.28 X (farther from stress-free temperature), while temperature increases the TTF value by a factor of ~107.

5.12 BEoL Failure Mechanisms – Aluminum Stress Migration (Al SM) (cont'd)

5.12.4 Examples of aluminum stress migration



(a) metal lines with Al SM voids



(b) higher magnification of Al SM voids

Figure 5.12-1 — Examples of aluminum stress migration

5.13 BEoL Failure Mechanisms – Copper Stress Migration (Cu SM)

Due to the combination of different materials and process temperatures used in chip fabrication, the Cu lines in advanced Cu technologies exist in a state of tensile stress **[5.13.1]**. When geometric configurations produce local peaks in stress and when such a peak exists at a location of marginal adhesion or at a preexisting process-induced void, large stress gradients are created. The term stress migration (stress-induced voiding, or simply stress voiding) refers to the movement of metal atoms under the influence of such a mechanical stress gradient. Little metal movement (migration) occurs until the stress exceeds the yield-point of the metallization. Then atoms diffuse from sites of low stress into regions of high stress and contribute to void growth, and when the void is large enough, the void can cause an electrical open or sufficient resistance increase to interfere with chip functionality **[5.13.1 to 5.13.6]**.

Because Cu has a greater elastic modulus, greater melting point and greater yield strength, it is able to withstand stress better than Aluminum metallization. While the activation energy for Cu diffusion is larger than that for Al atoms (smaller relative diffusivity as temperature decreases), electrodeposited Cu has a much greater initial void concentration. Thus, with decreasing dimensions and the introduction of new materials, Cu has shown vulnerability to stress migration, just as its predecessor, Al, exhibited. Phenomenologically, SM in Cu occurs very similarly to that in Al. It is still a diffusive process and still depends on the magnitude of tensile stress in Cu. But because of differences in microstructure and fabrication methods, the number and location of stress-induced voids is very different from those in Al metallizations **[5.13.3, 5.13.5, 5.13.6]**.

5.13.1 Constraints and limitations

No agreed upon standard industry test for SM presently exists. The more common practice is to subject wafers containing test structures found sensitive to SM to elevated temperatures (150 °C to 300 °C) for extended times (~1000 hour), periodically cooling the wafers to room temperature to be tested for any increases in resistance **[5.13.1 to 5.13.5]**.

5.13 BEoL Failure Mechanisms – Copper Stress Migration (Cu SM) (cont'd)

5.13.1 Constraints and limitations (cont'd)

In contrast to Al metallizations, long serpentines of Cu at widths <2 μm are not sensitive to SM. Instead, a variety of specialized structures involving vias contacting a line or plate from above have shown sensitivity to SM, indicating that proximity of large Cu reservoirs and poor or non-existent contact between via liner and that of the metal below are important factors **[5.13.1, 5.13.3]**. SM voiding under vias contacting narrow dual-damascene Cu lines has been associated with delayed grain growth in the bottoms of the trenches. Additional grain growth takes place during baking and generates additional vacancies that can contribute to void growth **[5.13.1]**.

SM depends on both mechanical stress and on temperature. Mechanical stress that is caused by differences in the thermal expansion coefficients between Cu and the surrounding liners and dielectric, increases at lower temperatures. The atomic mobility, which depends on the diffusivity, increases at higher temperature. A maximum in void growth rate therefore occurs at an intermediate temperature where the product of the stress and the diffusivity is at a maximum. For Cu, the temperature of maximum void growth is generally in the range of 175 °C to 225 °C **[5.13.1]**.

Some studies of Cu stress voiding show no maximum in void growth, but rather seem to indicate a continuing increase in growth rate with increasing temperature (no stress dependence). This may be because insufficiently high temperatures were used during stress, or because another factor, such as delayed grain growth, is an important contributor **[5.13.2]**.

Because the mechanical stress is temperature dependent, a straightforward determination of the diffusional activation energy is difficult to obtain. In the absence of other data, an E_{aa} value of ~0.9 eV, the same as for EM, can be used, but values ranging from 0.74 to 1.2 eV have been reported **[5.13.1, 5.13.2]**.

The effects of SM in Cu metallizations is most severe under vias contacting wide lines **[5.13.1, 5.13.3]**.

5.13.2 Models

5.13.2.1 Thermomechanical stress model

The time-to-failure (TTF) can use an Eyring model, for which one computes the product of a power-law on mechanical stress and an Arrhenius factor. If the stress is generated by differing thermal expansion rates, then the stress is called "thermomechanical stress" and is proportional to the change in temperature. Attention should be given to ensuring TTF is calculated only for similar geometries since geometric factors were simplified out of the equations.

Therefore, the time-to-failure can be written **[5.13.1, 5.13.5]**:

$$TTF = B_o * (T_o - T)^{-N} * \exp(E_{aa} / kT) \qquad \textbf{(5.13.1)}$$

where

- B_o = pre-factor
- T_o = stress-free temperature for metal (approximate metal deposition temperature for copper)
- N = 2 to 4 for ductile metals
- E_{aa} = apparent activation energy, 0.9 eV for interfacial diffusion (Cu-cap interface)
- k = Boltzmann's constant
- T = temperature in kelvin

5.13 BEoL Failure Mechanisms – Copper Stress Migration (Cu SM) (cont'd)

5.13.3 Stress migration numerical example

Objective: Calculate the acceleration factor (AF) for stress migration in an office environment vs. an accelerated stress environment.

Assumptions:
Office conditions are: 50 °C chip temperature inside the enclosure
Accelerated conditions are: 150 °C stress temperature
T_o = 300 °C
N = 3.0
E_{aa} = 0.9 eV

AF, the ratio of the time-to-failure (TTF) values will be:

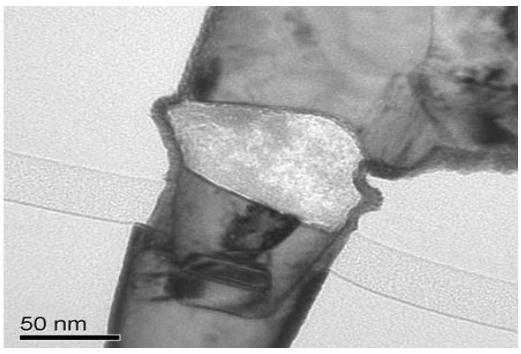
$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = [(T_o - T_{office}) / (T_o - T_{accel})]^{-N} * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{accel})]$$

$$AF = [(300 - 50) / (300 - 150)]^{-3.0} * \exp[(0.9 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 50)\text{K} - 1 / (273 + 150)\text{K})]$$

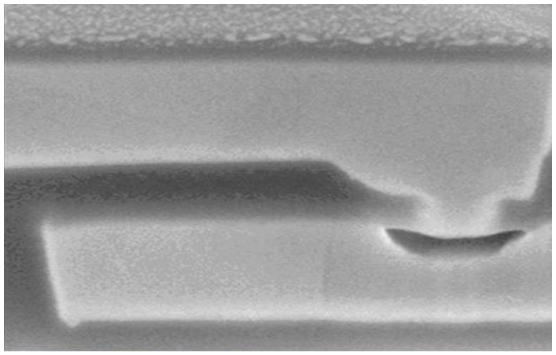
$$AF = 0.216 * 2.08 \times 10^3 = 450$$

Conclusion: Moving from the accelerated environment to the office environment will increase TTF value to about 450-fold that of the accelerated stress value. Mechanical stress decreases the TTF value by ~0.22 X (farther from stress-free temperature), while temperature increases the TTF value by a factor of ~2080.

5.13.4 Examples of copper stress migration



(a) stress-induced void in Cu via over line



(b) stress-induced void in Cu line under via

Figure 5.13-1 — Examples of copper stress migration

5.14 Packaging/Interfacial Failure Mechanisms – Fatigue failure due to temperature cycling and thermal shock

Fatigue failure can occur in ULSI devices due to temperature cycling and thermal shock. Permanent damage accumulates during thermal cycling or temperature shock. Damage from thermal cycling can also accumulate each time the device undergoes a normal power-up and power-down cycle. Such cycles can induce a cyclical stress that tends to weaken materials **[5.14.1 to 5.14.15]**, and may cause a number of different types of failures, including:

- Dielectric/thin-film cracking
- Lifted bonds
- Fractured/broken bond wires
- Solder fatigue (joint/bump/ball)
- Cracked die or molding compound
- Delaminated die
- Lifted die

Solder connections are particularly common and important as they can fatigue to failure under thermomechanical stress, commonly driven by mismatch in thermal expansion coefficient and Young's modulus. Solder connections are commonly used inside IC components, for example C4s (a.k.a. Controlled Collapse Chip Connnection, patented in 1969 by LF Miller of IBM) or second level solder connections betweeen IC components and printed circuit boards (PCB, a.k.a. PWB or Printed Wire Boards).

5.14.1 Constraints and limitations

"Linearity" is assumed, i.e., modeling parameters are constant over the range of interest (stress vs. customer application).

Alternative methods are needed for reliability estimates (AF or FITs) under certain conditions such as:

- Temperature cycle range crosses a critical temperature such as T_g (glass transition temperature of the polymer).
- Material property changes dramatically over the temperature range of interest. For example, the stress relaxation rate of Pb-based solders changes substantially near room temperature (see note below).

5.14.2 Models

5.14.2.1 Coffin-Manson model [5.14.1 to 5.14.4]

For ductile materials, low cycle fatigue data are described well by the Coffin-Manson equation:

$$N_f = A_o * (1 / \Delta\varepsilon_p)^B \qquad \textbf{(5.14.1)}$$

where

N_f = number of cycles to failure
A_o = material dependent constant
$\Delta\varepsilon_p$ = plastic strain range, which is the difference in strain per cycle (unit-less)
B = empirically determined constant

Low cycle fatigue is defined as a stress condition in which some hundreds or thousands of cycles cause failure, while high cycle fatigue would require millions of cycles. The Coffin-Manson model was originally developed for ductile materials (iron and aluminum alloys for aircraft), but has been successfully applied to brittle materials as well.

5.14 Packaging/Interfacial Failure Mechanisms – Fatigue failure due to temperature cycling and thermal shock (cont'd)

5.14.2 Models (cont'd)

5.14.2.2 Modified Coffin-Manson model [5.14.1, 5.14.3]

The Coffin-Manson equation works well, even for brittle material failures, where failure is dominated by crack initiation and growth, rather than simple plastic deformation. During a temperature cycle, not all of the stress (temperature range, ΔT) may be inducing plastic deformation. If a portion of the cycle, ΔT_o, is actually elastic, then the elastic portion should be subtracted from the total strain range.

$$\Delta\varepsilon_p \propto (\Delta T - \Delta T_o)^B \quad \textbf{(5.14.2)}$$

Note that geometric factors relating to strain are simplified out of the equation thereby eliminating prediction to other geometries or material properties and liming use performance enveloping. Therefore, for temperature cycling or thermal shock with plastic deformation, the Coffin-Manson equation becomes:

$$N_f = C_o * (\Delta T - \Delta T_o)^{-q} \quad \textbf{(5.14.3)}$$

where

N_f = number of cycles to failure
C_o = material dependent constant
ΔT = entire temperature cycle-range for the device
ΔT_o = portion of the temperature range in the elastic region
q = Coffin-Manson exponent, an empirically derived constant, unique to each failure mechanism

It is noted that if the elastic range (ΔT_o) is much smaller than the entire temperature cycle range (ΔT), then it may be dropped without significant error being introduced (usual practice). Thus,

$$N_f = C_o * (\Delta T)^{-q} \quad \textbf{(5.14.4)}$$

The solution applies to similar form-factors only due to elimination of geometric parameters. Most failure mechanisms will show the same failure rate for slow temperature cycling and for rapid thermal shock, but solder fatigue is a significant exception. Low melting point solders are used at temperatures in excess of $T_{melting}$ / 2, so creep is significant and the mechanical properties are extremely temperature and time-sensitive. Conversely, strain rate for brittle materials (those with large q values) seems to be largely irrelevant.

Table 5.14-1 — Values for q for common ULSI material classes [5.14.6].

Material	q
ductile metal, e.g., solder	1-3
hard metal alloys/intermetallics (e.g., Al-Au)	3-5
brittle fracture (e.g., Si and dielectrics : SiO_2, Si_3N_4)	6-9

5.14 Packaging/Interfacial Failure Mechanisms – Fatigue failure due to temperature cycling and thermal shock (cont'd)

5.14.2 Models (cont'd)

5.14.2.3 Norris Landzberg model [5.14.9, 5.14.15]

The Norris Landzberg modification of the Coffin-Manson approach adds additional multiplicative terms relevant to solder joint fatigue. These additional terms factors are a cyclic frequency factor as a power law and an Arrhenius-like temperature dependence. It should be noted that by using this approximation, temperatures must be expressed in °K.

Using equation **(5.14.4)** and applying Norris Landzberg modifications, the acceleration factor, AF for conditions in stress and the field is as follows:

$$AF = (\Delta T_{stress} / \Delta T_{field})^n * (f_{field} / f_{stress})^m * \exp[(E_{aa} / k)(1 / T_{max,field} - 1 / T_{max,\ stress})] \quad \textbf{(5.14.5)}$$

where

- E_{aa} = apparent activation energy in eV/atom for physics units or Kcal/mole for chemical units, typically 0.122 for SnPb solder and 0.188 for SAC solder
- n = material dependent constant, typically 1.9 for SnPb solder and 2.65 for SAC solder
- m = material dependent constant, typically 1/3 for SnPb solder and -0.136 for SAC solder
- ΔT = temperature cycle-range
- T_{max} = maximum temperature of the temperature cycle-range (°K)
- f = cyclic frequency factor (i.e. per day, so 2 stress cycles per hour would have an f_{stress} value of 2 * 24 = 48)
- k = Boltzmann's constant, 8.62 x 10^{-5} eV/kelvin

Note: In some works, the values of m for SnPb are reported as -1/3 because f_{stress} has been placed in the numerator instead of the denominator. This would give a value of 0.136 for SAC solder.

5.14.3 Temperature cycling numerical example

Objective: Calculate the acceleration factor (AF) for wire bond intermetallics due to temperature cycling in an office environment compared to an automotive environment.

Assumptions:
Office conditions are: once daily temperature swings of 20 °C
Automotive conditions are: 4 cycles per day with a swing of 80 °C
$\Delta T >> \Delta T_o$
q = 4

Using equation **(5.13.3)**, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } N_f \text{ values per stress cycle, office/automotive)} = (\Delta T_{office} / \Delta T_{auto})^{-q}$$

$$AF = (20 / 80)^{-4}$$

AF (office/automotive per cycle) = 256 per cycle, but more cycles/day for automotive also

Conclusion: So, a comparative evaluation of the automotive environment to office environment would show a TTF value 1000-fold that of the automotive value, of which 256-fold is due to the temperature excursion difference, while 4 X is due to cyclic frequency.

5.14 Packaging/Interfacial Failure Mechanisms – Fatigue failure due to temperature cycling and thermal shock (cont'd)

5.14.4 Preferred model and rationale

If a critical temperature is crossed during each temperature cycle, at least four different approaches can be used.

The preferred approach is to calculate AF and FITs for each zone where the modeling parameters are constant. Using available data **[5.14.4, 5.14.7, 5.14.8]**, the Coffin-Manson exponent can be allowed to vary between the high and low temperature zones. Most materials have a constant Coffin-Manson exponent, but Pb-based solders are the conspicuous exception because use temperatures are well above the homologous temperature at which creep and massive diffusion starts to occur.

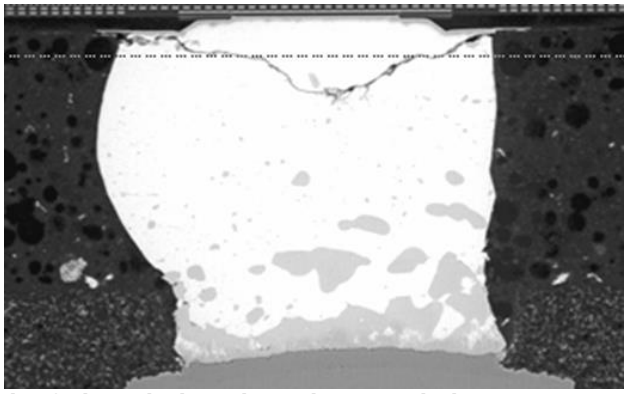
The most commonly used method utilizes a Coffin-Manson exponent weighted over the temperature range.

Another alternative is to use the Norris-Lanzberg approach **(see 5.14.2.3)**, which adds additional multiplicative terms. The factors are a cyclic frequency factor as a power law (typically with an exponent of 1/3) and a mild exponential temperature Arrhenius-like dependence (typically using an "apparent activation energy" of ~0.1 eV and the highest vs. lowest cyclic temperature.

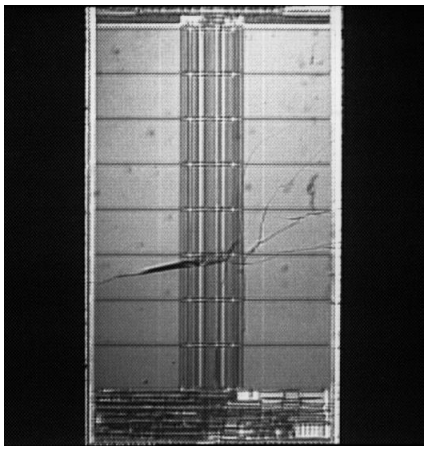
Another method, but the most labor-intensive, is to use Finite Element Analysis (FEA) to derive the von Mises stress (driver for shear & metal deformation) or maximum principal stresses (driver for cracking and fracture) to feed the simple Coffin-Manson equation **(5.14.1)**. Caveat: FEA results are very sensitive to mesh size, so comparisons must maintain same mesh size at the critical sites.

5.14 Packaging/Interfacial Failure Mechanisms – Fatigue failure due to temperature cycling and thermal shock (cont'd)

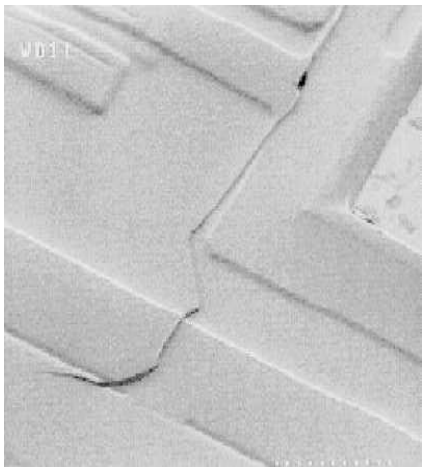
5.14.5 Examples of fatigue failure



(a) ductile solder fatigue-induced crack network due to temperature cycling



(b) brittle failure (Si fracture) due to temperature cycling



(c) brittle failure (top-side passivation fracture)

Figure 5.14-1 — Examples of temperature cycling/thermal shock damage

5.15 Packaging/Interfacial Failure Mechanisms – Interfacial failure due to temperature cycling and thermal shock

Interfacial failure can occur in ULSI devices after temperature cycling and thermal shock **[5.15.1 to 5.15.3]**. Interfacial failure **[5.15.5]** can include:

"Popcorn" is defined as an audible fracture of the interface between molding compound and a Si chip or its leadframe or substrate, commonly due to insufficient interfacial adhesion, especially if moisture is present. This failure mechanism is usually modeled by means of elastic beam bending which can be solved in closed form. Delamination of the metal/dielectric stack on the Si chip (BEoL) or inside a substrate, e.g., a printed circuit board used for flip chip products or for grid array products (Ball GA, Pin GA, Land GA). One must comprehend the stress (or stress-intensity factor) needed to propagate cracks at the relevant interfaces and moisture diffusivity kinetics (Relative Humidity, Temperature & time) to the relevant interfaces. Kinetics are often modeled as a Paris power-law on stress **[5.15.7 to 5.15.9]** or as the Energy Release Rate **[5.15.4 to 5.15.6]** as a function of crack size and stress-intensity factor.

Film crazing can occur in brittle dielectric films, especially when a brittle film is under hydrostatic tensile stress, as the total energy of the component might be smaller if the energy associated with new free surfaces being created is less than the strain energy density integrated over the volume of the strain field. The same interplay of free surface energy vs. that in the strain field is relevant to interfacial crack propagation as well. Crazing kinetics are often modeled as a Paris power law on stress or as the Energy Release Rate as a function of crack size and stress-intensity factor.

Wire bonds can be "lifted" (wire and intermetallic compound disconnected from the bonding pad) if temperature cycling produces progressive delamination of the molding compound from the Si chip surface. Wire bonds can also break above the ball in "bamboo" fashion under temperature cycle if the wire grain size is too large. This issue has been solved for a long while by adding Group II impurities to the Au wire and by avoiding high CTE silicone die coats. These mechanisms are well modeled by Coffin-Manson or Paris power law models.

Silicon chip fracture under temperature cycling can occur if insufficiently slotted Al lines exist at the edge of large chips and the fracture propagates through the metal/dielectric stack into bulk silicon. Silicon chip fracture can also occur if die attach voids exist near the chip edges. These mechanisms are well modeled by Coffin-Manson.

5.15.1 Constraints and limitations

"Linearity" is assumed, i.e., modeling parameters are constant over the range of interest (stress vs. customer application).

Alternative methods are needed for reliability estimates (AF or FITs) under certain conditions such as:

- Temperature cycle range crosses a critical temperature such as T_g (glass transition temperature of the polymer).
- Material property changes dramatically over the temperature range of interest. For example, the stress relaxation rate of Pb-based solders changes substantially near room temperature.

5.15 Packaging/Interfacial Failure Mechanisms – Interfacial failure due to temperature cycling and thermal shock (cont'd)

5.15.2 Models

5.15.2.1 Paris Law model

The Paris Law is based on a fracture mechanics approach when it was first proposed by Paris and Erdogan in 1963 **[5.15.7 to 5.15.9]**. The Paris Law models the log of the crack propagation rate vs. log of stress-intensity factor, typically finding three regimes: zone I represents sub-critical crack initiation; zone II represents subsonic velocity; zone III represents near sonic crack growth. The Paris Law exponent varies widely from one zone to another and among the materials within a given zone.

Paris Law **[5.15.7]** is used to characterize sub-critical crack growth under fatigue loading based on a power-law and is expressed as follows using the stress-intensity factor:

$$da / dN = C * (\Delta K)^m \quad \textbf{(5.15.1)}$$

or alternatively using the energy release rate instead of the stress-intensity factor:

$$da / dN = C * (\Delta G)^m \quad \textbf{(5.15.2)}$$

where

a = crack size
N = number of load cycles
ΔK = range of stress intensity factor per cycle
ΔG = range of energy release rate per cycle
C, m = material specific coefficients or exponents

Table 5.15-1 — Values for the Paris Law exponent, m for several different interfacial fracture mechanisms

Materials	Paris Exponent	Source
Cu to polymer	3.5	**[5.14.11]**
Au_4Al Intermetallic Fracture in wire bonds	4	**[5.14.2]**
Low-k ILD to Cu	4	**[5.14.12]**
Au downbond Heel Crack	5	**[5.14.15]**
Alumina substrate fracture	5.5	**[5.14.15]**
Interlayer Dielectric Cracking	5.5	**[5.14.16]**
Multilayer FR4 Printed circuit board	6.9	**[5.14.12]**
Silicon fracture	7	**[5.14.1]**
Cratered Si beneath wire bond pads	7.1	**[5.14.2]**
Thin-Film Cracking, aka Silicon fracture	8.4	**[5.14.3]**

5.15 Packaging/Interfacial Failure Mechanisms – Interfacial failure due to temperature cycling and thermal shock (cont'd)

5.15.3 Paris Law model numerical example

Objective: Calculate the acceleration factor (AF) for delamination of molding compound from Si chip (low-k or FTEOS vs. Cu) in an office environment compared to an automotive environment.

Assumptions:
Office conditions are: once daily temperature swings of 20 °C
Automotive conditions are: 4 cycles per day with a swing of 80 °C
Follows Paris Law using energy release rate; note: $dN \propto (\Delta G)^{-m}$
m = 4

Using equation **(5.14.2)**, the ratio of the time-to-failure (TTF) values will be:

$$\text{AF (ratio of dN / da values per stress cycle, office/automotive)} = (\Delta G_{office} / \Delta G_{auto})^{-m}$$

$$\text{AF} = (20 / 80)^{-4}$$

AF (office/automotive per cycle) = 256 per cycle, but more cycles/day for automotive also

Conclusion: So, a comparative evaluation of the automotive environment to office environment would show a TTF value 1000-fold that of the automotive value, of which 256-fold is due to the temperature excursion difference, while 4 X is due to cyclic frequency.

5.15.4 Example of interfacial failure

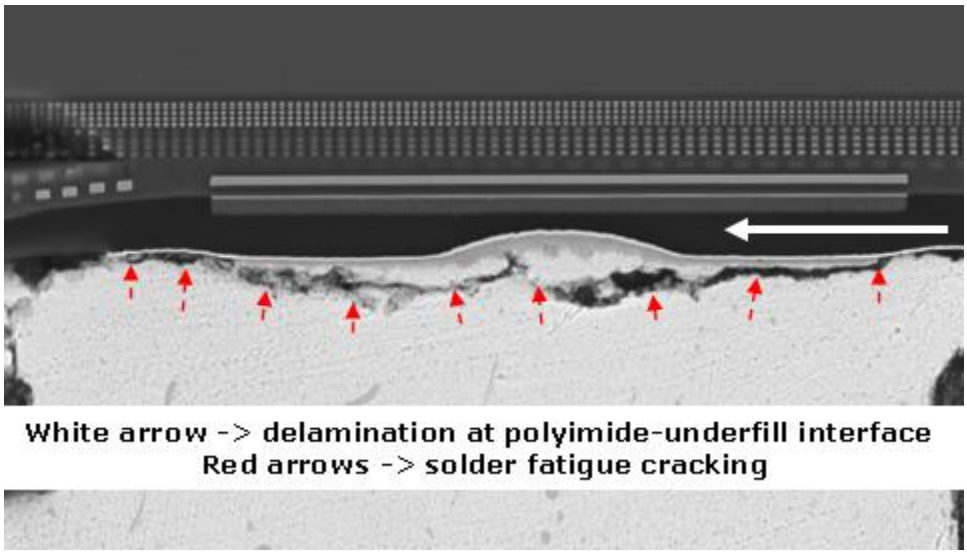


Figure 5.15-1 — Example of interfacial delamination after temperature cycling
(also shows a solder fatigue crack).

5.16 Packaging/Interfacial Failure Mechanisms – Intermetallic and oxidation failures due to high temperature

Intermetallic compound formation can occur in ULSI devices due to bake or due to the high temperature end of temperature cycling or thermal shock **[5.16.1 to 5.16.24]**. This failure mechanism can produce wire bonds or C4 bumps (Controlled Collapse Chip Connection) with excessive electrical resistance and poor mechanical properties (low strength and brittle fracture). Intermetallic growth kinetics and oxidized film thickness are well modeled by an Arrhenius equation and an activation energy.

Intermetallic growth can also impair solderability and contact resistance. Contact resistance can also be impaired by leadfinish oxidation. Oxidation is well modeled by an Arrhenius equation and an activation energy as well.

While many failure mechanisms are thermally activated, it is important to realize that each mechanism will have a unique (apparent) activation energy.

5.16.1 Constraints and limitations

"Linearity" is assumed, i.e., modeling parameters are constant over the range of interest (stress vs. customer application).

Alternative methods are needed for reliability estimates (AF or FITs) under certain conditions; for example, if the bake temperature crosses a critical temperature such that the failure mechanism and/or its activation energy changes.

Gaseous ambient can affect kinetics if Au-Al bonds can be isolated from oxygen or if hydrogen is present, as in a hermetic package. This is not an issue for plastic packages as gas diffusivity (moisture, oxygen, etc.) is large enough that the die surface will equilibrate with the ambient in a few months at room temperature, but much faster if warm or hot.

5.16.2 Models

5.16.2.1 Arrhenius models

Many thermally activated processes are modeled well by the Arrhenius equation:

$$\text{Rate} = R_o * \exp(-E_{aa} / kT) \qquad \textbf{(5.16.1)}$$

or

$$\text{Rate} = R_o * \exp(-E_{aa} / RT) \qquad \textbf{(5.16.2)}$$

where

- R_o = rate constant characteristic of infinite temperature
- E_{aa} = apparent activation energy in eV/atom for physics units or Kcal/mole for chemical units
- k = Boltzmann's constant, 8.62×10^{-5} eV/kelvin
- R = Rydberg gas constant, 23,063 cal/mole-kelvin
- T = temperature in kelvins

5.16 Packaging/Interfacial Failure Mechanisms – Intermetallic and oxidation failures due to high temperature (cont'd)

5.16.2 Models (cont'd)

5.16.2.2 Acceleration factor derived from Arrhenius model

The fundamental basis for themal activation is based on the probability of ascending a potential energy barrier due to the Maxwell-Boltzmann energy distribution. This physical explanation was actually anticipated by Arrhenius' work on chemical reaction rates, for which one would simply substitute the Rydberg Gas Constant for the Boltzmann Constant and use different units. We have chosen to use "physics" based units here; sometimes you will find two different versions for activation energy in chemical units. The equivalence is 23.1 kcal/mole K = 96.4 kJ/mole K = 1 eV/atom.

Using equation **(5.15.1)**, the acceleration factor, AF for T_1 vs. T_2 is as follows:

$$AF = \exp[(E_{aa} / k)(1 / T_1 – 1 / T_2)] \quad \textbf{(5.16.3)}$$

where

E_{aa} = apparent activation energy in eV/atom
k = Boltzmann's constant
T_1 = smaller temperature in kelvins
T_2 = larger temperature in kelvins

It is noted that the acceleration factor will be extremely sensitive to the value for the apparent activation energy, E_{aa}, and the temperature difference.

5.16.3 Arrhenius model numerical example

Objective: Calculate the acceleration factor (AF) for a "Severe Industrial" environment, considering only the hot 105 °C portion for 4600 hours and NOT considering the additional 20 years at 85 °C. Contrast the "Severe Industrial" environment to a "qualification" environment consisting of a bake for 1000 hours at 175 °C.

Assumptions:
Severe Industrial environment: 4600 hours at 105 °C chip temperature (T_1)
Qualification environment: 1000 hours at 175 °C (T_2)
E_{aa} = 1.1 eV

Using equation **(5.16.3)**:

$$AF = \exp[(E_{aa} / k)(1 / T_1 – 1 / T_2)]$$

$$AF = \exp[(1.1 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 105)\text{K} – 1 / (273 + 175)\text{K})]$$

AF (temperature only, not including 4600 vs. 1000 hours) = 195

AF (qualification / severe industrial) = (1000 / 4600) * 195 = 42

Conclusion: So, a comparative evaluation of the "qualification" environment to a "Severe Industrial" environment would show a time-to-failure (TTF) value 42-fold that of the "Severe Industrial" value, of which 195-fold is due to the temperature difference, while 4.6 X is due to the difference in time.

5.17 Packaging/Interfacial Failure Mechanisms – Tin Whiskers

Tin whiskers can create shorts between leads if they become longer than lead (pin) spacing (space applications are particularly vulnerable). The driving environmental factors for tin whisker growth have not been characterized until recently. However, the driving force from a metallurgical point of view is known to be compressive stress in the tin and many other factors. A comprehensive discussion of current tin whisker theory can be found in JP-002 **[5.17.10]**.

Tin Whisker formation on plated and soldered surfaces is a large reliability risk that allows for conductive metal single crystals to grow from the base over time in nearly all operating environments ranging from low humidity and temperature (space application) to 60 °C/93%RH conditions. The physical model used to explain this whisker initiation is based on **[5.17.7]**. Conductive crystals can grow to lengths that allow for contact of adjacent leads or break off and are transferred on to board and component locations that result in device failure in the field. Refer to the FAQ section of the NASA Tin Whisker website *http://nepp.nasa.gov/whisker/index.html* for information.

The mechanisms by which tin whiskers grow have been studied for many years. A single accepted explanation of the mechanisms has NOT been established. Some theories suggest that tin whiskers may grow in response to a mechanism of stress relief (especially "compressive" stress) within the tin plating. Other theories contend that growth may be attributable to recrystallization and abnormal grain growth processes affecting the tin grain structure (which may or may not be affected by residual stress in the tin plated film).

In the case of stress within the tin plating, there are some commonly accepted factors that can impart additional residual stress:

- Residual stresses within the tin plating caused by factors such as the plating chemistry and process. Electroplated finishes (especially "bright" finishes) appear to be most susceptible to whisker formation reportedly because bright tin plating processes can introduce greater residual stresses than other plating processes.
- The diffusion of the substrate material into the tin plating (or vice versa) can lead to formation of intermetallic compounds (such as Cu_6Sn_5 for a Sn over Cu system) that alter the lattice spacing in the tin plating. The change in lattice spacing may impart stresses to the tin plating that may be relieved through the formation of tin whiskers.
- Externally Applied Compressive Stresses such as those introduced by torque applied to a nut or a screw
- Bending or Stretching of the surface after plating (such as during lead-formation prior to mounting of an electronic component)
- Scratches or nicks in the plating and/or the substrate material introduced by handling, probing, etc.
- Coefficient of Thermal Expansion Mismatches between the plating material and substrate
- Corrosion and/or Oxidation – additional work in this area is currently underway.

5.17.1 Constraints and Limitations

Universal models predicting tin whisker time-to-failure have proven elusive due to the strong dependency of observed whisker growth on lead geometry, lead composition, temperature, RH (Relative Humidity), plating additives, internal stress, current density, plating temperature, post-plating anneal present or absent, Ni underlayer present or absent, etc.

The theory of whisker formation has no universal agreement other than that surface and subsurface stresses play a major role in the formation of these single crystal whisker structures and that the alloying of lead has the ability to minimize the whisker formation. Controversies regarding this model still exist. Hence users are encouraged to review literature before they make their own decisions for their unique technologies.

5.17 Packaging/Interfacial Failure Mechanisms – Tin Whiskers (cont'd)

5.17.1 Constraints and Limitations (cont'd)

Pb additive to Sn is known to reduce tin whisker jeopardy, as Pb changes mechanical behavior, i.e., Pb provides greater intrinsic creep rate, Pb reduces yield stress and Pb mitigates impurity effects on mechanical behavior. In addition, Pb segregates at interfaces, which increases grain boundary mobility, improves efficiency of grain boundary and surface sources as sinks for vacancies in creep, improves continuity of surface oxide, and changes IMC morphology

Pb changes electrodeposition behavior by increasing grain nucleation rate during electrodeposition and Pb provides electrolytes to create deposits with smaller organic and inorganic impurity levels.

5.17.2 Time to Whisker Nucleation Model

Although tin whisker time-to-failure models have not been established, a pre-cursor model, time-to-whisker-nucleation (TTWN), or whisker incubation time in hours, has been proposed **[5.17.7 to 5.17.9]**. However, care should be taken in the use of this model to ensure its applicability:

$$TTWN = A * \exp (E_a/(kT)) * \exp(C*RH) \quad \textbf{(5.17.1)}$$

where

A = constant, dependent upon materials & process details (hrs)
C = humidity coefficient
RH = Relative Humidity (%)
E_a = activation energy (eV)
k = Boltzmann's constant (eV/K)
T = temperature (K)

The above model (and its corresponding constants shown in Table 6-1) was collected from a variety of experiments performed on plastic packages with Matte Tin plating on top of a Copper Alloy (C194) leadframe with a 1-hour post-plating anneal of 150C within 24 hours of plating. Other models may apply to differing material compositions, process flows, plating chemistries, equipment, etc. Alternative models should be supported by empirical data and mutually accepted by customer and supplier. Further, this model does not specifically address mechanisms for whisker growth due to thermal cycling.

5.17.3 Tin Whisker Nucleation Numerical Example

Although the above model can be used to estimate time-to-whisker-nucleation, more effective use of the model can be made through the correlation of experimental data to field use conditions through the use of a calculated acceleration factor.

Objective: Calculate the acceleration factor (AF) for tin whiskers for an office environment vs. an accelerated environment

Assumptions:
Assume office (field) conditions defined as: 30 °C/40%RH for a chip, and whisker testing was performed at 60 °C/87%RH. Using values from Table 5.17-1 of A = 0.014hrs, Ea = 0.41eV, and C = -0.012:

$$TTWN_{modelexp} = A * \exp (E_a/(kT)) * \exp(C*RH)$$
$$= 0.014 * \exp(0.41/(8.62x10^{-5} * 333)) * \exp(-0.012*87)$$
$$= 7908.55 \text{ hrs}$$

5.17 Packaging/Interfacial Failure Mechanisms – Tin Whiskers (cont'd)

5.17.3 Tin Whisker Nucleation Numerical Example (cont'd)

$TTWN_{modelfield} = A * \exp(E_a/(kT)) * \exp(C*RH)$
$= 0.014 * \exp(0.41/(8.62x10^{-5} * 303)) * \exp(-0.012*40)$
$= 57204.77$ hrs

AF, the ratio of the time-to-whisker-nucleation (TTWN) values will be:

$AF = TTWN_{modelexp} / TTWN_{modelfield}$
$= (57204.77 / 7908.55)$
$= 7.23$

Alternatively, one can use the reduced form of the equation to determine the individual contributions from moisture and humidity:

$AF \text{ (ratio of } TTF_{modelfield} \text{ to } TTF_{modelexp} \text{ values)} = \exp[-C(RH_{field} - RH_{exp})] * \exp[(E_a / k)(1 / T_{field} - 1 / T_{exp})]$
$AF = \exp[-0.012(40-87)] * \exp[(0.41 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 30)K - 1 / (273 + 60)K)]$
AF = 1.76 (Humidity AF) * 4.12 (Temperature AF) = 7.23 (Overall AF)

Conclusion: So, moving from the accelerated environment to the office environment will increase TTWN value to 7.23 times the accelerated stress value due to temperature and humidity difference.

Table 5.17-1 — Values for the Time-To-Whisker-Nucleation model for various conditions

Plating	Corrosion?	Reflowed?	A (hrs)	Ea (eV)	C
3 μm	N	N	1.15	0.31	-0.031
10 μm	N	N	1.16	0.28	-0.017
10 μm	N	Y	0.014	0.41	-0.012
3 μm	Y	N	5.16	0.23	-0.018
10 μm	Y	N	1.16	0.28	-0.017
10 μm	Y	Y	1.97	0.3	-0.031

5.17 Packaging/Interfacial Failure Mechanisms – Tin Whiskers (cont'd)

5.17.4 Examples of Tin Whiskers (Annex A references in brackets)

Figure 5.17-1 — SEM of Tin Whiskers on Matte Tin plated Alloy 42 leads [5.17.4]

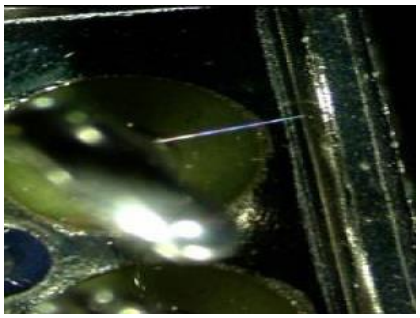


Figure 5.17-2 — Optical Image of a Tin Whisker growing from Relay lead to case [5.17.3]

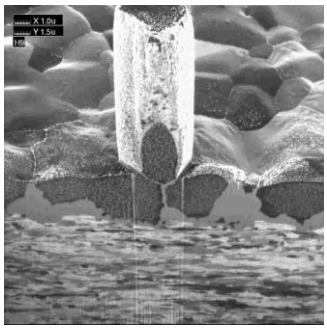


Figure 5.17-3 — FIB - matte tin whisker structure from a temperature cycled specimen [5.17.5]

Figure 5.17-4 — Optical Image - Tin Whisker growing from SAC 305 solder over Alloy 42 - matte tin [5.17.4]

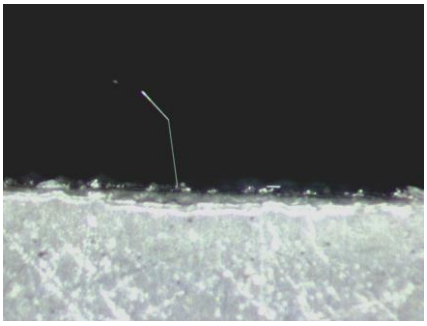


Figure 5.17-5 — Optical image of Tin Whisker on a copper coupon with matte tin plating [5.17.4]

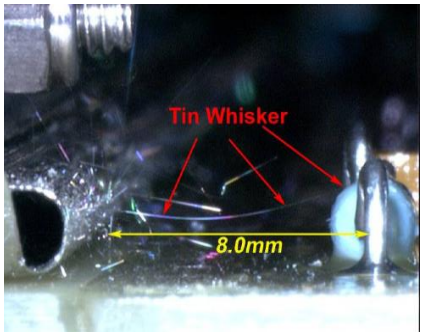


Figure 5.17-6 — 8 mm long Tin Whisker growing from a bracket holding electronics in a frame. The electronics were saved by having conformal coating on in this case, but this only protects from debris and does not stop growth **[5.17.3]**

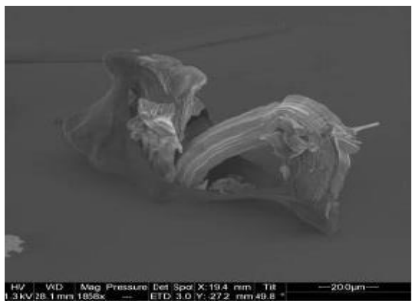


Figure 5.17-7 — Tin Whisker breaking through 10 μm Uralane 5750 coating (9 yr office storage) [5.17.3]

5.18 Packaging/Interfacial Failure Mechanisms – Ionic Mobility Kinetics (PCB) - Component Cleanliness

Each step of the component fabrication process has an impact on the surface contamination of the active component. The amount of ionic residue found on a finished device can be primarily attributed to the external wet chemical processing steps, for a QFP, DIP, SIP, BGA or chip package. After the molding encapsulation process, the surface plating and rinsing steps have the greatest impact on the component lead cleanliness. These wet chemical processes are using primarily the Methane Sulfonic Acid (MSA) electrolyte standard for plating the tin and tin lead finishes for the last 20 years. **[5.18.1]** Then each uses an alkaline neutralizing step to react the acid, followed by a water rinse. This wet chemistry process is a defining factor in the component cleanliness and if the MSA or alkaline neutralizer is not completely removed, these residues will cause electrical leakage and electrochemical migration corrosion issues. We must address a new-definition of Cleanliness **[5.18.2]**.

5.18.1 Constraints and limitations

Most of the literature is phenomenological rather than model-based. However, some data were found to support Arrhenius modeling vs. temperature for Ag and Mo migration as a function of temperature. One would expect an electric field or voltage-dependence for ionic mobility, but those data proved difficult to find. A much more thorough survey of the literature is needed to gather activation energy values for a wider variety of ions as a function of purity and other factors.

5.18.2 Arrhenius Model

$$TTF = A_0 \exp(-C*RH) * \exp (E_{aa}/kT) \qquad \textbf{(5.18.1)}$$

where

- A_o = arbitrary scale factor, dependent upon materials & process details
- C = sensitivity parameter for Relative Humidity
- RH = Relative Humidity in %, N/A for this failure mechanism
- E_{aa} = apparent activation energy, typically expressed in eV
- k = Boltzmann's constant
- T = temperature in kelvins

5.18.3 Ionic Mobility Numerical Example

Objective: Calculate the acceleration factor (AF) for Ag ionic mobility for an office environment vs. an accelerated environment

Assumptions:
Office conditions defined as: 50 °C chip temperature (inside a desktop PC) an estimate for activation energy for Ag migration is 1.12 eV based on [5.**18.10, 5.18.11, and 5.18.12**]
Accelerated condition: 60 °C
Activation energy, E_{aa}: 1.12 eV

AF, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = \exp[(E_a / k)(1 / T_{office} – 1 / T_{accel})]$$

$$AF = \exp[(1.12 \text{ eV} / 8.62 \times 10^{-5} \text{ eV/K})(1 / (273 + 50)\text{K} – 1 / (273 + 60)\text{K})]$$

$$AF = 3.3$$

Conclusion: So, moving from the accelerated environment to the office environment will increase TTF value to 3.3 times the accelerated stress value due to temperature difference.

5.18 Packaging/Interfacial Failure Mechanisms – Ionic Mobility Kinetics (PCB) - Component Cleanliness (cont'd)

5.18.4 Examples of Ionic Mobility

Typical contaminates found on finished components by Ion Chromatography are MSA, chloride, bromide, sulfate, phosphate, sodium and ammonia (when using a heated liquid extraction) per the IPC TM 650.2.3.28 test method. When any one of these or the collective combination is high electrical leakage and electrochemical migration problems will occur under ambient temperature and humidity conditions with powered assemblies.

Since 60-75% of the electronic assembly industry uses a no clean assembly technology approach, the incoming component cleanliness is now more critical than ever. With the no clean assembly process there is no post assembly cleaning is done to remove any detrimental residues. If components are high in corrosive / moisture absorbing residues then after the soldering operation they are still high in these residues.

Problems that occur with high levels of fabrication residue on the component

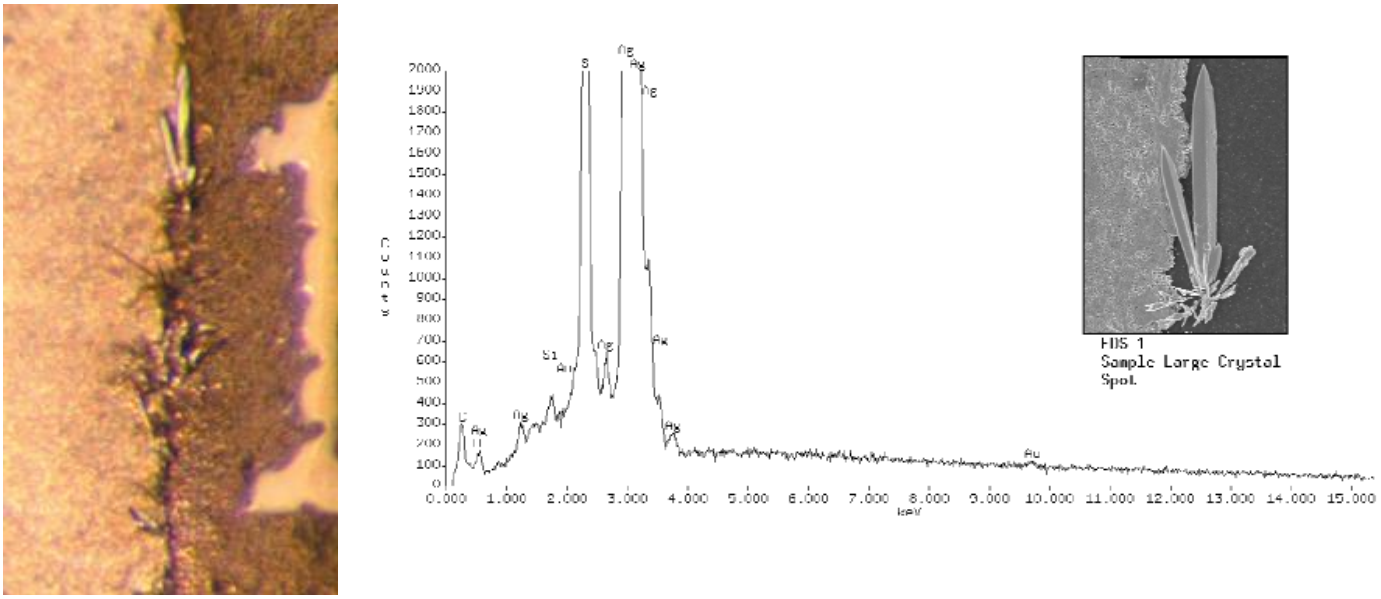


Figure 5.18-1 — Resistor corroded open due to trapped MSA residues in epoxy surface [3]

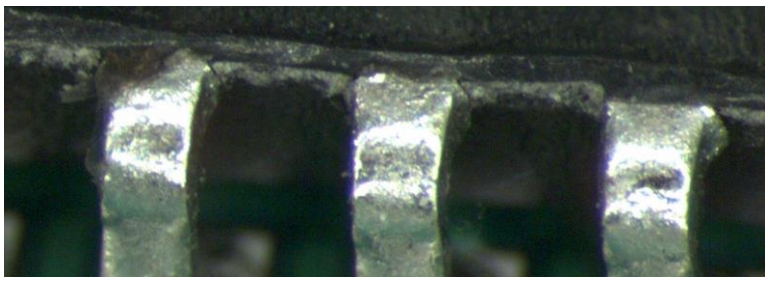


Figure 5.18-2 — Electrochemical migration between leads on a QFP

5.18 Packaging/Interfacial Failure Mechanisms – Ionic Mobility Kinetics (PCB) - Component Cleanliness (cont'd)

5.18.4 Examples of Ionic Mobility (cont'd)

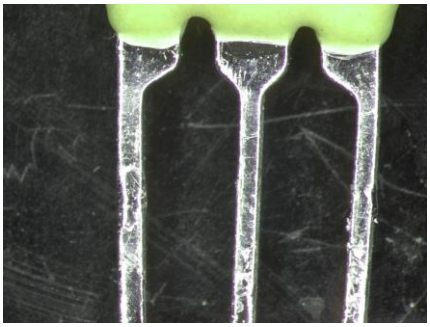


Figure 5.18-3 — Leakage and corrosion problems with residues on tinned leads due to aggressive flux

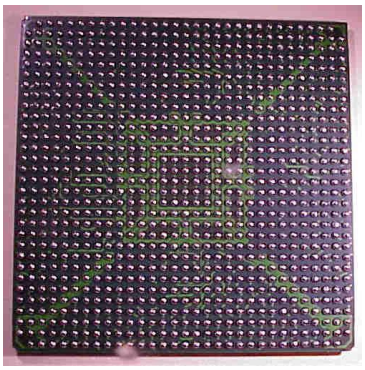


Figure 5.18-4 — Leakage and corrosion problems with BGA components between balls due to poorly cleaned water soluble solderpaste from ball attachment

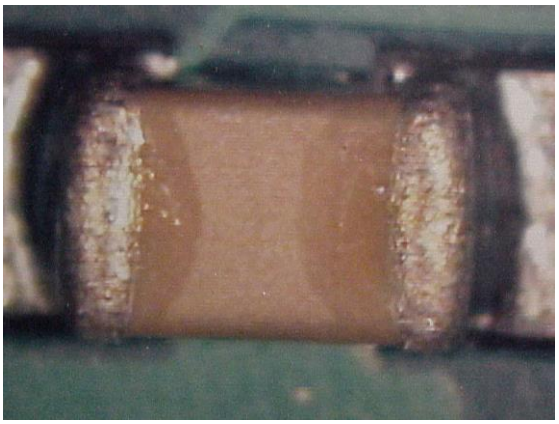


Figure 5.18-5 — Leakage due to large MSA levels on Chip capacitor
Sulfate levels of 24 μg/in^2 (~4 μg/cm^2) [5.18.5]

5.19 Reliability data/analysis

5.19.1 Failure distributions

The lognormal and Weibull distributions are most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate is a special cases of the Weibull. Under specific condition ($\beta \approx 3.4$), Weibull can also approximate a normal distribution. It is important to note that distribution shape can be used to infer whether the failure mechanism is defect-controlled or intrinsic (defect-free). Clearly an important objective to know whether defects are present or not, as defect presence would affect the corrective action plan. Extrapolation of large failure rates seen under stress to ppm in the user environment will be strongly affected depending on whether one uses the Weibull or lognormal distribution. We will provide guidance on how one can know which distribution is more effective and accurate. The Probability Density Function (PDF) and Cumulative Distribution Function (CDF) for the lognormal, Weibull, and exponential distributions are described below along with several key characteristics for each distribution.

5.19.1.1 Lognormal distribution

$$f(t, t_{50}, \sigma) = (1 / \sigma\, t) * [1 / \sqrt{(2\pi)}] * \exp\{-0.5 * [\ln((t / t_{50}) / \sigma)]^2\} \quad \textbf{(5.19.1a)}$$

CDF:

$$F(t, t_{50}, \sigma) = \Phi[\ln(t / t_{50}) / \sigma] \quad \textbf{(5.19.1b)}$$

where

t = time under stress
t_{50} = time to 50% cumulative fail
σ = shape parameter

The lognormal distribution is specified by two parameters: the median time-to-failure t_{50} and the shape parameter sigma (σ). The shape parameter σ is approximately equal to $\ln(t_{50} / t_{16})$. The lognormal distribution is often used to model cumulative degradation process, e.g., electromigration.

NOTE The lognormal distribution can also be characterized by a three parameter lognormal distribution and electromigration has been shown to fit this scenerio. The third parameter is a time scale shift.

5.19.1.2 Weibull distribution

PDF:

$$f(t, t_{63}, \beta) = (\beta / t_{63}) * (t / t_{63})^{\beta-1} * \exp[-(t / t_{63})^{\beta}] \quad \textbf{(5.19.2a)}$$

CDF:

$$F(t, t_{63}, \beta) = 1 - \exp[-(t / t_{63})^{\beta}] \quad \textbf{(5.19.2b)}$$

where

t = time under stress
t_{63} = time to 63.2% cumulative fail
β = shape parameter

The Weibull distribution **[5.19.3]** is specified by two parameters: the characteristic life t_{63} and the shape parameter beta (β). The value of the shape parameter determines whether the failure rate is increasing ($\beta > 1$), decreasing ($\beta < 1$), or constant ($\beta = 1$). If $\beta \sim 3.4$, the Weibull distribution approximates the normal distribution. It is often used to model failures due to “weakest link”, e.g., dielectric breakdown.

NOTE A three parameter Weibull may also be used. The third parameter is a time scale shift.

5.19.1 Failure distributions (cont'd)

5.19.1.3 Discussion of the lognormal and Weibull distributions

Figure 5.18-1 shows failure rate vs time relative to the time for 50% failure for several values of the lognormal sigma (0.1 to 1.0),

where

$$\text{lognormal } \sigma \approx \ln(t_{50} / t_{16}) \qquad \textbf{(5.19.3)}$$

The pdf was normalized for each of the sigma values so that one can see how the shape of the curve changes with sigma value. As sigma is a measure of time dispersion, it should be no surprise that the smallest sigma value has the narrowest width in the chart. Each increase in sigma value broadens the time distribution for the fails, which entails a nasty consequence for a customer, namely early (and continuing failures). Inspection of Figure 5.19-1 shows that sigma values near unity (and the red danger flag) exhibit considerable pdf before t_{50}. Thus, the job of the reliability, the process and the design engineers is to develop strategies to make sigma as small as possible, with a large t_{50} also, or equivalently that Weibull β be as large as possible.

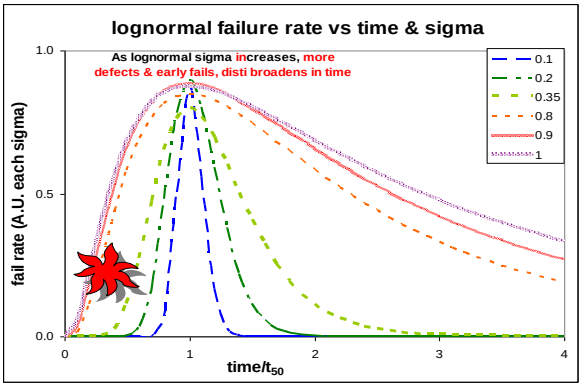


Figure 5.19-1 — Lognormal Distribution

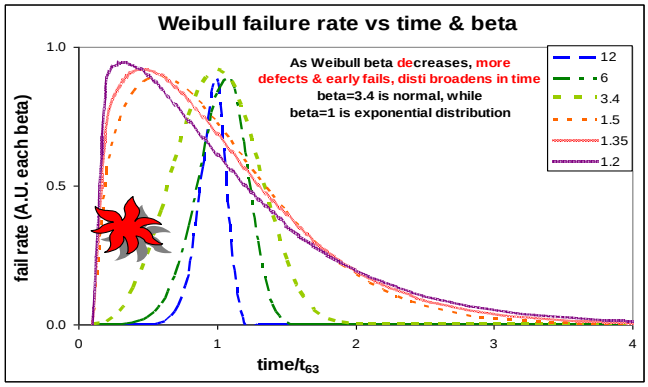


Figure 5.19-2 — Weibull Distribution

Figure 5.19-2 shows pdf value for several values of the Weibull shape parameter.

The pdf was normalized for each of the Weibull β values so that one can see how the shape of the curve changes with β value. Each decrease in β value produces a nasty consequence for a customer, namely early (and continuing failures). Inspection of Figure 5.19-2 shows that small Weibull shape factor (β) values (near the red danger flag in Figure 5.19-2) exhibit considerable pdf rate before t_{63}. Thus, the job of the reliability, the process and the design engineers is to develop strategies to make sigma as small as possible. Naturally one needs a large t_{50} also, but small σ values are even more important. A good rule of thumb regarding interpretation of the σ value is: a σ value < ~½ is usually indicative of an intrinsic failure mechanism, while a σ value > ~1 is usually indicative of a defect-controlled failure mechanism. Good products (free of defects, suffering only intrinsic failure) will exhibit small lognormal σ values.

It is noteworthy that Figure 5.19-1 and Figure 5.19-2 look similar, which is a deliberate effort to show that either distribution can be used for reliability engineering, especially for deciding whether the failure mechanism is defect-controlled or intrinsic (defect-free). The reason that these charts look so similar was based on an 1996 IRPS Tutorial in which its author showed that Weibull β (shape factor) and lognormal σ are the inverse of one another. Unfortunately, the tutorial had a slight numeric error (commonly encountered in TDDB work) regarding base 10 vs. natural logarithms, for which the conversion factor is 2.3:1 because ln(10) = 2.3. Thus,

$$\text{lognormal } \sigma \approx 1.2 / \beta \qquad \textbf{(5.19.4)}$$

5.19.1 Failure distributions (cont'd)

5.19.1.3 Discussion of the lognormal and Weibull distributions (cont'd)

As you may note, the lognormal sigma values in Figure 5.19-1 (0.1, 0.2, 0.35, 0.8, 0.9 & 1.0) are equivalent (in terms of time dispersion) to the Weibull shape factors in Figure 5.19-2 (β = 12, 3, 3.4, 1.5, 1.35 and 1.2). A good rule of thumb regarding interpretation of the Weibull β value is: a Weibull β value > ~2.4 is usually indicative of an intrinsic failure mechanism, while a Weibull β value < ~0.8 is usually indicative of a defect-controlled failure mechanism. Good products (free of defects, suffering only intrinsic failure) will exhibit large Weibull β values.

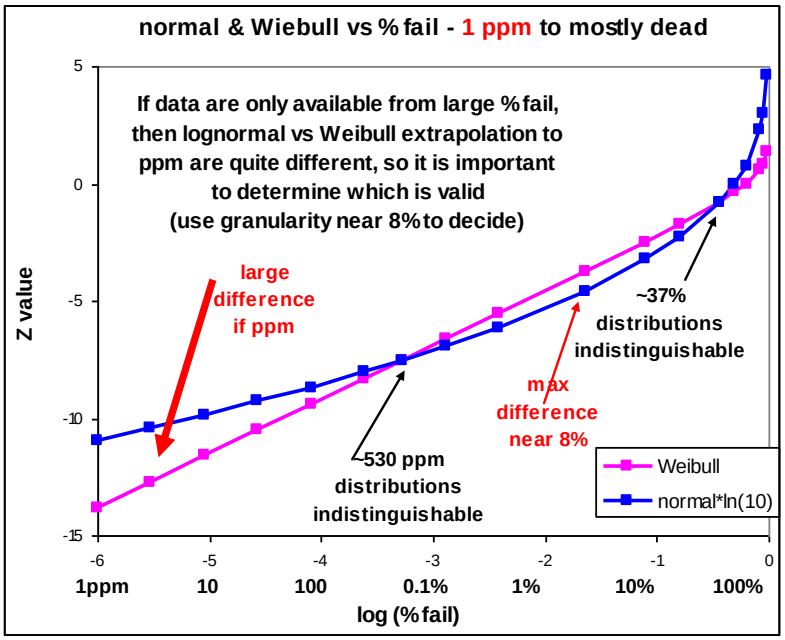


Figure 5.19-3 — Tracking of lognormal and Weibull distributions over range 1 ppm to 100%

Figure 5.19-3 was created independently of Wager's 1996 IRPS Tutorial, but has the same properties, now with modern formatting. The key points are that the curves cross each other twice, once near 37% and again near 530 ppm. There is a substantial divergence between the curves near ~8% fail and below 30 ppm. Accordingly, it is important to know which distribution is an accurate representation of the data. The most straightforward method to choose one distribution over the other would be to plot failure data on lognormal and on Weibull axes and see which regression fit has the best correlation coefficient. This author has never successfully put this idea into practice (correlation coefficients are usually very similar), but Figure 5.19-4 and Figure 5.19-5 will attempt to show why that method failed.

One can take advantage of the divergence near ~8% to try to learn which distribution is the better fit. If your failure data are mostly near ~10-37% fail, the divergence is small and the curvature of one distribution vs. the other is so small that you won't be able to make a choice. Practical sample sizes and coarse readout intervals usually don't produce the best data to make a choice.

5.19.1 Failure distributions (cont'd)

5.19.1.3 Discussion of the lognormal and Weibull distributions (cont'd)

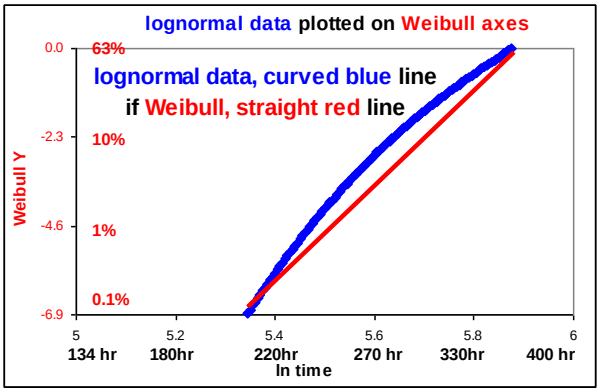


Figure 5.19-4 — Lognormal plotted as Weibull

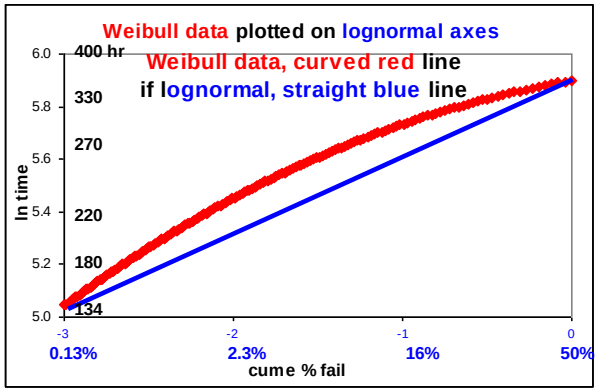


Figure 5.18-5 — Weibull plotted as lognormal

Figure 5.19-4 and Figure 5.19-5 show that if the governing distribution is plotted as the correct distribution (i.e., on the correct axes), then a straight line regression fit can be obtained. If the data show curvature, incorrect axes were chosen. Concave downward curvature can also indicate an incubation or initiation time, prior to which there are no failures. If this is the case, a 3-parameter Weibull or 3-parameter lognormal distribution may prove useful for analyzing the data.

Figure 5.19-4 was constructed in the following fashion. A perfect lognormal response was assumed, but Weibull axes are chosen producing a non-linear response, the curved blue line. If there were sufficient curvature on these axes (and correct sign), it would indicate that lognormal were a better fit to the data. We have assumed lognormal parameters were t_{50} = 365 hr and a lognormal sigma = 0.17 (time dispersion, i.e., $\sigma = \ln(t_{50} / t_{16})$). If one sees maximum dispersion of the curves near a few % fail, we would conclude that the data can be fitted by a lognormal distribution, the curved blue line.

Similarly, Figure 5.19-5 was constructed in the analogous fashion, but with lognormal and Weibull interchanged. A perfect Weibull response was assumed (% fail vs time). If there were sufficient curvature on these axes (and correct sign), it would indicate that Weibull were a better fit to the data. Assumed Weibull parameters were t_{63} = 377 hr and a Weibull beta of 5.89 (time dispersion). If one sees maximum dispersion of the curves near a few % fail, one would conclude that the data can be fitted by a Weibull distribution, the curved red line.

We can use the divergence and curvature to advantage if and only if we have copious data near ~8% fail (1.5 σ below t_{50}) such that we can discriminate between a straight line and a curve. Thus, in situ data (failure time of every unit known during stress) would be ideal, but one might be able to make the choice using more finely spaced readout intervals over the range –1 to –2 sigma below t_{50}.

In contrast to the curvature between lognormal and Weibull near ~8% cumlative failing the two distributions cross twice near 37% fail and near 530 ppm. Thus, if your objective is to project your data to proximity to these cummulative fail values, it will not be important whether you use Weibull or lognormal distribution.

There is one more important distinction to understand regarding Weibull vs. lognormal distributions. If you must predict failure rates deep into the ppm range one distribution will produce a very large difference from the other. For example, if the lognormal distribution were predicting the time to 1 ppm fail, Weibull would be predicting ~30 ppm (horizontal line in Figure 5.19-3). The difference is not so extreme if the lognormal distribution were used to predict the time to 100 ppm fail, as Weibull would be predicting ~300 ppm. Thus, the Weibull distribution will be pessimistic in the ppm range while lognormal will be optimistic.

5.19.1 Failure distributions (cont'd)

5.19.1.4 Exponential distribution:

PDF: $f(t) = (1 / MTTF) * \exp(-t / MTTF)$ **(5.19.5a)**

CDF: $F(t) = 1 - \exp(-t / MTTF)$ **(5.19.5b)**

where

t = time under stress
MTTF= Mean Time To Failure

The exponential distribution is specified completely by one parameter, called the mean-time-to-failure (MTTF). The exponential failure rate is 1 / MTTF which is also known as λ.

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant. The exponential distribution is the only one for which a MTTF (mean-time-to-failure) value may easily be estimated and it is simply the reciprocal of the failure rate (λ). In addition, it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The conventional chi-squared expression for failure rate, λ, is:

$$\lambda = \chi^2(2n + 2,1-\alpha) * 10^9 / (2 * ss * t * AF) \quad \textbf{(5.19.6)}$$

where

λ is the failure rate in FITs (failures per billion unit-hours)

$\chi^2(2n + 2,1 - \alpha) / 2$ is the upper confidence value for "n" failures and upper confidence limit, α (expressed as a decimal value)

ss is the sample size, t is the test duration in hours

AF is the total acceleration factor relating the life test conditions (junction temperature, voltage, etc.) to ~~an~~ the assumed field conditions

The χ^2 (chi-squared) value for 2n + 2 degrees of freedom and the probability, $1 - \alpha$, can be obtained from a table or calculated using Microsoft Excel chi-squared inverse function [=CHIINV(1–α,2n+2)].

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-part sample from a certain product population had one failure and a 60% confidence level was desired. The chi-square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the "true" value of the population's defect rate is between zero (or some very small value) and 2.02%.

If there are a number of failures at early read points, it would be prudent to attempt to determine the type of failure distribution. See a text on reliability engineering such as reference **[5.19.1]**. It is wise to repeat the test with more read-points or, if possible, monitored tests to detect the actual time of failure. If a large sigma is seen, the failures may well be due to a defective subpopulation, for which the data should be parsed for separate plots.

5.20 Design of Experiments (DOE) for determination of modeling parameters

If the modeling parameters for a particular failure mechanism are not available in the literature or from internal sources or the parameters (sensitivity factors such as activation energy, exponent value, etc) are uncertain, you will need to execute a Design of Experiments **[5.20.1]** to measure the appropriate constants. It is essential that a range of stress intensity values be used to produce a statistically significant number of failures at several different times for each stress condition (aim for 50% cum fail). If multiple failure modes and mechanisms are produced by the stress, the failures must be parsed and analyzed separately. Overstress conditions can be used to define technology margin (performance in excess of requirement) and acceleration factors.

For example, let's assume that your failure mechanism is thermally activated, for which the conventional model is that of Arrhenius. Thus, ln(rate) is proportional to $(E_{aa} / k)*(1 / T)$, where E_{aa} = activation energy, k = Boltzmann's constant, and T = absolute temperature. Plotting the data as ln(rate) vs. reciprocal temperature will produce a straight line (or one could perform an exponential regression line fit), if a single mechanism is present. In order to get a reasonably accurate E_{aa} value, your 1 / T values should be far enough apart to modulate the rate significantly (at least several-fold, preferably over as many orders of magnitude as you can manage). How much difference in temperature stress will be needed? Let's say you expect E_{aa} to be ~0.7 eV and the relevant temperature is near 100 °C. With those parameters every 20 °C change in temperature will change the rate by ~3-fold. Thus, ±20 °C will modulate the rate by ±3-fold. Similarly, every 40 °C change in temperature will change the rate by 9-fold. Thus, ±40 °C will modulate the rate by ±9-fold. From a statistical point of view the probability of detecting significant parameters can be increased if a plurality of the runs are at the minimum possible temperature and a similar plurality were the maximum possible temperature, reserving some samples for intermediate temperatures to check for “linearity” on the plot of 1 / kT vs. ln(rate).

As a second example, let's assume that your failure mechanism is some sort of mechanical fatigue, for which the conventional model is Coffin-Manson or Paris Law. Thus, rate (cycles-to-failure or time-to-failure) is proportional to $\text{strain}^{\text{exponent}}$ and the usual surrogate for strain is the swing in temperature (ΔT) between hot and cold in temperature cycling or thermal shock. Plotting the data as $\log(N_{50})$ vs log(ΔT) (or one could perform a power-law regression fit), for which the slope is the exponent (Coffin-Manson exponent, CM^, or PL^). How much temperature swing will be needed? Let's say you expect a Coffin-Manson exponent of 8 and the relevant temperature swing (ΔT) is 100 °C. If your experiment were to explore ΔT values half as large and twice as large as the nominal 100 °C, the failure rate would be modulated by 2^8 = 256-fold, which would provide more than sufficient failure rate change to determine the Coffin-Manson exponent. As above in the Arrhenius example, you want to perturb the rate by as much as possible without changing to a different failure mechanism (verified by failure analysis).

What if you don’t know the “threshold for pain,” that is the ΔT that would be needed to force a significant number of failures (aim for 50% fail)? Step stress is an effective technique to establish the “threshold for failure,” especially if the temperature cycle intervals (size of ΔT change per step), number of cycles and sample size are chosen intelligently. One could use **[5.15.15]** as a temperature cycling example of the step stress principle, while **[5.20.2]** describes the same idea applied to TDDB. One would make a guess as to the expected Coffin-Manson exponent (CM^) or Paris Law exponent (PL^) based on Table 5.14-1, or Table 5.15-1, or Table 6-1. One would compute an acceleration factor from step n to step n + 1, picking a ΔT value such that AF per step is ~2. For example, say you estimated that CM^ or PL^ were 8. Then you would want an interval of roughly 9% in ΔT per step to make each step twice as stressful as the preceeding. The reason to make each step twice as stressful as the preceeding is to make sure that cumulative strain prior to the lethal blow, the “backwards” sum of all cumulative strains,from beginning stress to the penultimate (failing) stress is small compared to the strain produced by the final failing stress. For this example, the “previous” cumulative strain would be 1/2 + 1/4 + 1/8 + etc, which sums to unity.

5.20 Design of Experiments (DOE) for determination of modeling parameters (cont'd)

Thus, the stress at the final step, where you finally provoked massive failure, is 50% of the total cumulative strain. Step stress sample size need be only 10-20 as you intend to provoke massive cumulative failure.

Similarly, the number of temperature cycles would be ~20, deliberately small to produce a cost-effective stress. This approach takes advantage of the power-law on ΔT rather than the more expensive (linear) time (number of cycles).

Having determined the "theshold for pain" at some particular ΔT value, you would subject a slightly larger sample size to a constant ΔT, but with a logarithmically increasing readout interval, such that you can generate a lognormal plot. A second set of samples (twice the sample size as the first set) would be subjected to a smaller ΔT (9% smaller ΔT for this example) and driven to massive failure, again with a logarithmically increasing readout interval, such that you can generate a second lognormal plot. Similarly, do the same for a third set of samples (quadruple the sample size, but 1/4 of the stress).

Table 5.20-1 — Example for temperature cycle schedule
(if CM^ or PL^ were ~8, number of cycles for each ΔT and sample size value)

Run #	ΔT °C	Sample Size	Read Out #1	Read Out #2	Read Out #3	Read Out #4	Read Out #5
1	180	50	10	20	40	80	160
2	162	100	20	40	80	160	320
3	144	200	40	80	160	320	640

Logarithmically increasing (cumulative) readout values span two orders of magnitude in "time" so we can estimate lognormal sigma or Weibull beta (shape factor), but equally important, deduce the N_{50} or N_{63} value.

Examine each lognormal plot to see if it is single mode or not (confirm with failure analysis). If multiple failure mechanisms are active, parse the data into homogeneous failure modes, extracting N_{50} (or N_{63}) and sigma (β) values for each one. The final activity is to plot log(N_{50}) vs log(ΔT) (either $\log_{10}$ or ln is okay) from which the slope of the fitted regression line (if log(ΔT) is the x-axis) is the desired CM^ or PL^.

As a third example, let's consider that your failure mechanism is electrically activated, perhaps something similar to TDDB, for which a conventional model is the "E model." Thus, ln(rate) is proportional to the difference in electric field ($\Delta V / t_{ox}$). Plotting the data as ln(rate) vs. $\Delta V / t_{ox}$ will produce a straight line (or one could perform an exponential regression fit), for which the slope is the γ value. How much modulation in $\Delta V / t_{ox}$ will be needed to modulate the failure rate significantly? Let's say you expect a γ value of 1 decade per MV/cm of electric field. Thus, changes in electric field of ± 1 MV/cm will modulate the failure rate by an order of magnitude. You might also want to modulate t_{ox} to see if the relevant stress is electric field or voltage and whether the functional dependence is power law or exponential. As above in the other examples, you want to perturb the rate by as much as possible without changing to a different failure mechanism.

As a fourth and final example, let's consider that your failure mechanism responds to two different stresses. For example, TDDB is sensitive to both temperature and voltage. The key design strategy is to assume that an Eyring model will work adequately (stresses are mathematically separable). You construct a "space" (temperature is one axis and voltage is the other) and make sure that your stress conditions explore a constrained area of that space, using factorial design. Your initial DOE might employ a 2x2 or 3x3 "box" or perhaps a box/star. A particularly good reference for all DOE, factorial design and statistics issues is "Statistics for Experimenters" by Box, Hunter & Hunter **[5.20.1]**. Software by JMP is also an effective tool for DOE.

6 Activation energies and model factors

Table 6-1 is a collection of failure mechanisms and the best available associated Apparent Activation Energies and Non-Arrhenius Model Parameters from a critical review of the literatute. These values may be used in the models presented in clause 4. A description of the column headings follows:

Failure Mode: a general description of the failure mode.

Failure Mechanism: a brief description of the mechanism.

E_{aa}: apparent activation energy for the mechanism in electronvolts (eV).

Note: The Annex A Citation suffix value supplies literature references in Annex A relating to activation energies and other modeling parameters.

Non-Arrhenius Model parameters: parameters for various models for other than thermal acceleration.

Type: model equation type -- power law or exponential

Varbiable: parameter involved in model

Units: Variable (parameter) units

Exponent: power exponent or exponential constant (see model applicable to failure mechanism).

6 Activation energies and model factors (cont'd)

Table 6-1 — Failure Mechanisms and Model Parameters
All models are inherently Eyring; so, take product of Arrhenius & other functions
NOTE Add Section Number to suffix find full citation (e.g., 2nd Gate short citation is: [5.1.26])

Sect.	Failure Mode	Failure Mechanism	Activation Energy	Non-Arrhenius Model Parameters				Annex A Citation Suffix
			E_{aa} (eV)	Type	Variable	Units	Parameter	
5.1	Gate short to source or drain	Intrinsic breakdown; for gate oxide thk >4 nm	0.7	Exponential	E	MV/cm	γ = 2.3 with γ = a/kT, a = 7.2 eA, T = 90 °C	1, 4, 5, 25
5.1	Gate short to source or drain	Intrinsic breakdown; for gate oxide thk 2-4 nm	N/A	Exponential	V	V	10	26
5.1	Soft breakdown between gate & source or drain	Percolation; for gate oxide thk <2 nm	N/A	Power	V	V	40	28, 30
5.2	Δg_m, Δspeed	HCI or CHC, n-channel	-0.2 to +0.4	Power	I_{sub}	μA	2-4	5
5.2	Δg_m, Δspeed	HCI or CHC, p-channel; for L >=250 nm	-0.1 to -0.2	Power	I_G	μA	2-4	1, 2, 3
5.2	Δg_m, Δspeed	HCI or CHC, p-channel; for L <250 nm	+0.1 to +0.4	Power	I_{sub}	μA	2-4	5
5.2	Δg_m, Δspeed	HCI or CHC; for effective gate ox thick <2 nm	Small, positive	Power	$1 / V_{CC}$	V^{-1}	40	16
5.2	Δg_m, Δspeed	HCI or CHC; injection of hot electrons or holes from channel into gate dielectric	-0.17	Exponential	$\Delta V / t_{ox}$	V/Å	α = 0.005	12
5.3	Δg_m, Δspeed	NBTI; non-dispersive H_2 transport	-0.02	Power	Volt	V	3-4	4, 14
5.3	Δg_m, Δspeed	NBTI; non-dispersive H_2 transport	0.55	Power	time	hr	1/6	18

6 Activation energies and model factors (cont'd)

Table 6-1 — Failure Mechanisms and Model Parameters (cont'd)
All these models are inherently Eyring; so, take product of Arrhenius & other functions
NOTE Add Section Number to suffix find full citation (e.g., 1st Mobile ion citation is: [5.4.4] & [5.4.5])

Sect.	Failure Mode	Failure Mechanism	Activation Energy	Non-Arrhenius Model Parameters				Annex A Citation Suffix
			E_{aa} (eV)	Type	Variable	Units	Parameter	
5.4	Mobile ions, ΔV_t	Na^+ diffusion thru silica	0.75	Conc. Grad.	Conc	cm^{-2}	1	4, 5
5.4	Mobile ions, ΔV_t	H_2 , H^+ diffusion thru silica	0.42, 0.70	Conc. Grad.	Conc	cm^{-2}	1	5, 8
5.4	Mobile ions, ΔV_t	Diffusion thru silica: large [Na] concentration	1.8	Conc. Grad.	Conc	cm^{-2}	1	4,5
5.4	Mobile ions, ΔV_t	Diffusion thru silica: small [Na] concentration	0.75	Conc. Grad.	Conc	cm^{-2}	1	4,5
5.4	Mobile ions, ΔV_t	Diffusion thru silica: other alkali/alkaline earth ions	>1	Conc. Grad.	Conc	cm^{-2}	1	4,5
5.4	Mobile ions, ΔV_t	K^+ diffusion thru silica	1.03, 1.09	Conc. Grad.	Conc	cm^{-2}	1	5, 9
5.4	Mobile ions, ΔV_t	Ca^{++}, Ba^{++}, Mg^{++} diff. SiO_2	1.27,1.4,1.59	Conc. Grad.	Conc	cm^{-2}	1	5
5.4	ΔV_t	Diffusion; surface charge on glassivation	1.13	N/A	N/A	N/A	N/A	6
5.5	Charge loss	Charge hopping	0.6	Exponential	V_G	V	0.25	7
5.5	Charge loss	Tunneling due to SILC	0-0.27	Exponential	V_T	V	2.2-5.9	1, 8
5.5	Charge loss/gain	Dielectric detrapping	1.1-1.2	N/A	N/A	N/A	N/A	5, 6, 7
5.5	Charge gain	Single bit charge gain, (tunneling from SILC) in FGMs	0.18	Exponential	V_G	V	4-4.6	9
5.6	Charge loss	Dispersive charge spreading	0.75 + 0.07 * log(# p/e cycles)	N/A	N/A	N/A	N/A	2,3
5.7	Resistance decrease	GST re-crystallization	2.5	N/A	N/A	N/A	N/A	6,8,10-14

6 Activation energies and model factors (cont'd)

Table 6-1 — Failure Mechanisms and Model Parameters (cont'd)
All these models are inherently Eyring; so, take product of Arrhenius & other functions
NOTE Add Section Number to suffix find full citation (e.g., 1st Short, leakage citation is: [5.7.3] & [5.7.5])

Sect.	Failure Mode	Failure Mechanism	Activation Energy	Non-Arrhenius Model Parameters				Annex A Citation Suffix
			E_{aa} (eV)	Type	Variable	Units	Parameter	
5.8	Short, leakage	TDDB; traps & percolation	0.75	Exponential	E	MV/cm	4	3, 5
5.8	Short, leakage	Cu ion drift	1.0	Conc. gradient	Conc	cm^{-2}	1	10
5.9	Open	Al EM; vacancy transport	0.8	Power	J	A/cm^2	2	2, 7, 11, 17
5.9	Open	Al EM; grain-boundary diffusion	0.68	Power	J	A/cm^2	2	18, 19
5.9	Open	Al EM; interfacial diffusion	0.95	Power	J	A/cm^2	2	18, 19
5.10	Open	Cu EM; vacancy transport	0.9	Power	J	A/cm^2	1.1	3
5.11	Open	Al corrosion (Chloride)	0.75	Power	RH	%	2.7	8
5.11	Open	Al corrosion (Chloride)	0.75	Exponential	1/RH	$\%^{-1}$	529%	15
5.11	Open	Al corrosion (Phos Acid)	0.3	Exponential	1/RH	$\%^{-1}$	300%	7
5.11	Open	Al corrosion (Chloride)	0.75	Exponential	RH	%	0.12 $(\%)^{-1}$	10
5.11	Leakage	Diffusion thru passivation cracks	0.79	Power	RH	%	4.64	23
5.11	Open	Ion transport thru PolyImide	1.15	Power	RH	%	0.98	23
5.11	I_{cc} quiescent	Water diffusion	0.73	Power	RH	%	1	20
5.11	Leakage	Ionic conductivity – lead frame coplanarity tape 1	0.74	Power	RH	%	12	24
5.11	Leakage	Ionic conductivity – lead frame coplanarity tape 2	0.77	Power	RH	%	5	24
5.12	Open	Al stress migration – vacancy diffusion & drift – voids coalesce	0.6 gb 1.0 bamboo	Power	Mech Stress	Pa	2-3	2, 3
5.12	Open	Al stress migration – vacancy diffusion & drift – voids coalesce	0.6 gb 1.3 intra-grain	Power	ΔT (T_o - T) T_o = zero stress temp	ºC	2-3	2, 3
5.13	Open	Cu stress migration – vacancy diffusion & drift – voids coalesce	0.74-1.2 for Cu-cap interface - strong fcn of interface prep	Power	ΔT (T_o - T) T_o = zero stress temp	ºC	2-4	1, 5
5.14	Open	Crack propagation - stress concentration in PbSn solder fatigue if >30C	N/A	Power	ΔT (T_{hi} - T_{lo})	ºC	2.7	4
5.14	Open	Crack propagation - stress concentration in PbSn solder fatigue if <30C	N/A	Power	ΔT (T_{hi} - T_{lo})	ºC	1.2	4
5.14	Open	Crack Propagation – Fatigue SnAg solder	N/A	Power	ΔT (T_{hi} - T_{lo})	ºC	2.3	13
5.14	Open	Al wire	N/A	Power	ΔT (T_{hi} - T_{lo})	ºC	3.5	12
5.14	Open	Au_4Al IMC	N/A	Power	ΔT (T_{hi} - T_{lo})	ºC	4	3
5.14	Open	Crack Propagation – Fatigue SnPb solder	0.122	Power	$\Delta T_{test}/\Delta T_{field}$ f_{field}/f_{fest}	N/A	1.9 1/3	9, 15
5.14	Open	Crack Propagation – Fatigue SAC solder	0.188	Power	$\Delta T_{test}/\Delta T_{field}$ f_{field}/f_{fest}	N/A	2.65 -0.136	16

6 Activation energies and model factors (cont'd)

Table 6-1 — Failure Mechanisms and Model Parameters (cont'd)
All these models are inherently Eyring; so, take product of Arrhenius & other functions
NOTE Add Section Number to suffix find full citation (e.g., 1st Crack propagation citation is: [5.13.4])

Sect.	Failure Mode	Failure Mechanism	Activation Energy	Non-Arrhenius Model Parameters				Annex A Citation Suffix
			E_{aa} (eV)	Type	Variable	Units	Parameter	
5.15	Cu to polymer	Interfacial delamination	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	3.5	11
5.15	Au_4Al intermetallic	Fracture beneath wire bond	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	4	2
5.15	Low-k ILD to Cu	Delam driven by ERR	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	4	12
5.15	Au downbond heel crack	Fracture near IMC	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	5	15
5.15	Broken alumina	Fractured bubble memory substrate	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	5.5	15
5.15	Delamination	Interfacial dielectric cracking	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	5.5	16
5.15	Delamination	FR4/PCB adhesion driven by ERR	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	6.9	12
5.15	Non-functional	Silicon fracture	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	7	1
5.15	Open	Cratered Silicon beneath wire bond pads	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	7.1	2
5.15	Non-functional	Thin-film cracking, aka Silicon fracture	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	8.4	3
5.16	Open	Delamination of mold compound from chip	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	3.5-5.1	24
5.16	Open	IMC, Kirkendall voiding	1.0-1.9 strong fcn of impurity & conc.	N/A	N/A	N/A	N/A	15
5.16	Open	IMC, Kirkendall voiding	1.26	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	4	8, 13, 14, 23
5.16	Open	Metallization ductility driven by epoxy mismatch	N/A	Power	$\Delta T (T_{hi} - T_{lo})$	^oC	6.3	3
5.17*	Shorts	Tin whisker growth	0.28	Exponential	C A	$\%^{-1}$ hr	-.012 0.014	7
5.18	Shorts	Ag ion mobility	1.11					10,12
5.18	Shorts	Mo ion mobility	1.06					6

***** A more comprehensive table of constants is listed in section 5.17.3. Note that alternate constants and/or models may be necessary; these should be supported by empirical data and mutually agreed upon by the customer and supplier.

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Annex B (informative) – JEP122 Revision History

B.1 Differences between JEP122H and JEP122G

The following list briefly describes most of the changes made to entries that appear in this publication, JEP122H, compared to its predecessor, JEP122G (October 2011).

Section	Description of change
All	Added a space between the degree sign and the number, e.g., 50 °C.
Foreword	Added Oxford Commas.
Introduction	Added “Apparent” for activation energies.
3.3	Removed revision letters and dates
5	Added Lawson model in Section 5.11
5	Added Norris-Landzberg model in Section 5.13.
5	Added distributed NVM cycling model in section 5.5 and additional text to Mechanisms affecting data retention (5.5.5.1).
Annex A	Added new references 5.14.15, and 5.5.12-21.

B.2 Differences between JEP122G and JEP122F

The following list briefly describes most of the changes made to entries that appear in this publication, JEP122G, compared to its predecessor, JEP122F (March 2009).

Section	Description of change
3	In 3.2, removed “phase change” as this revision has the inclusion of PCM memory
5	In 5.5.2.2, added charge detrapping model extension to NAND Flash
5	In 5.6.1, removed last paragraph
5	Added new 5.7 and subclauses
5	Renumbered old clauses 5.7 thru 5.19 to 5.8 thru 5.20
6	In Table 6.1 added 5.7. Failure Mode
6	In Table 6.1 changed Sect. references 5.7 thru 5.17 to 5.8 thru 5.18
Annex A	Added new reference 5.5.7
Annex A	Renumbered old references 5.5.7 thru 5.5.10 to 5.5.8 thru 5.5.11
Annex A	Added new section for “GST-PCM NVD (5.7.1 thru 5.7.14)
Annex A	Renumbered old references 5.7.x thru 5.19.x to 5.8.x thru 5.20.x

B.3 Differences between JEP122F and JEP122E

Revision F provides a major re-write to section 5.5 and adds new sections 5.16 (PCB ionic mobility) and 5.17 (tin whiskers). Previous sections 5.17 and 5.18 are renumbered to 5.18 and 5.19.

Page	Description of change
iii, 5	Deleted note about “Sum of Failures” method (introduction, Terms and definitions)
1	Add g) Tin Whiskers and g) Printed Circuit Board Ionic Mobility (Scope)
4	Define Whisker and PCB cleanliness (Terms and definitions)
6	Updated what is not included, aka plans for future revisions (3.2)
7	Add JESD 88, Dictionary of Terms (3.3)
22-25	Major revision to Floating Gate Flash memory section (5.5)
62-64	New section on Tin Whisker Growth Kinetics (5.16)

Annex B – (informative) List of references (cont'd)

B.3 Differences between JEP122F and JEP122E (cont'd)

65-67	New section on Ionic Mobility Kinetics for PCB (5.17)
79	Added two model parameter datasets (for 5.16 and 5.17)
76-79	Changed "exponent" to "parameter" (6)
84	Added one new floating gate Flash memory reference (for 5.5.8)
92-93	Added references for new sections, tin whiskers and PCB ionic mobility (for 5.16 and 5.17)

B.4 Differences between JEP122E and JEP122D

Page	Description of change
1	Additional notes added to the acceleration factor definition
2	Additional notes added to the acceleration factor, temperature definition
2	Note added to the definition of activation energy (E_a)
2	The apparent activation energy (E_{aa}) definition has changed with several notes added
3	The definition of activation energy, planning (E_{ap}) has been changed with notes added
3	Additional notes added to the definitions of failure mechanism, failure mode, & failure rate
3	The definition for random defect has been changed.
3	A note has been added to the relative humidity (RH) definition
4	A definition for sum-of-the-failure-rates method has been added
5	Added new Section 3 and renumbered succeeding sections
9	Revised 5.1, TDDB gate oxide, was 4.3
14	Revised 5.2, HCI, was 4.4
17	Revised 5.3, NBTI, new
20	Revised 5.4, Mobile Ions, was 4.5
22	Revised 5.5, Polysilicon gate NVD, new
25	Revised 5.6, ONO gate NVD, new
28	Revised 5.7, TDDB, ILD-Low k-Cu, new
36	Revised 5.8, Al Electromigration, was 4.1
39	Revised 5.9, Cu Electromigration, new
42	Revised 5.10, Al Corrosion, was 4.2 and added Cu corrosion (new)
46	Revised 5.11, Al Stress Migration, was 4.6
49	Revised 5.12, Cu Stress Migration, new
52	Revised 5.13, Fatigue failure, was 4.7
55	Revised 5.14, Interfacial failure, new
58	Revised 5.15, Intermetallic and oxidation failures, new
60	Revised 5.16, Reliability data/analysis, was 4.8
65	Revised 5.17, DOE for modeling parameters, was 4.9
67	Revised section 6, modeling parameters for acceleration factor parameters in view of reorganization
72	Reorganized Annex A, reference list, in view of new order and new sections
84	Deleted Annex B, as it was consolidated with Annex A and renamed Annex C as Annex B

B.5 Differences between JEP122D and JEP122C

Page	Description of change
1	**acceleration factor (*A*):** Changed definition to align with JESD91A
1	**activation energy (E_a):** Changed definition to align with JESD91A
1	**apparent activation energy (E_{aa}):** Changed definition to align with JESD91A
29	Annex A: Renumbered to begin at 1.

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